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Development and production:

Introduction

The ATCA-IO-PROCESSOR blade is designed for Fast Control and Data Acquisition Systems. It is compatible with PICMG 3.0/3.4 and AXIe specifications, comprises a passive RTM for rear IO connectivity to ease hot-swap maintenance and simultaneously to increase cabling life cycle. Also includes PICMG 3.0/3.4 redundancy support, in order to provide high levels of system reliability and availability.

Is a high channel number IO board with galvanic isolation and FPGA based processing. Simultaneously digitized data from all ADCs of the board can be filtered/decimated in the FPGA, decreasing data throughput, increasing ADC resolution, and sent through PCI Express to multi-core processors in the ATCA shelf hub slots. Concurrently the multi-core processors can update the board DACs in real-time. Full-duplex point-to-point communication links between all FPGAs, of peer blades inside the shelf, allow the implementation of distributed algorithms and MIMO systems. Support for several Timing and Synchronization architectures is provided.

Some key features:

1. Onboard ADC or DAC modules (or a combination of both) with galvanic isolation;
2. Xilinx Virtex 6 FPGA;
3. DDR3 SODIMM memory;
4. CompactFLASH memory card;
5. Intelligent Platform Management Controller;
6. Two PCI express ×4 (generation 2) ATCA Fabric channels (dual-star topology support);
7. Eleven Xilinx Aurora ×1 (or other ATCA compatible communications protocol) ATCA Fabric channels (full-mesh topology support);
8. Two Fast Ethernet (IEEE1588-V2 and LXI compatible) ATCA Base channels (dual-star topology support);
9. Timing and Synchronization support.

Specifications

ATCA (PICMG 3.0/3.4)

- Node blade
- Single front slot and single RTM slot (IO on the rear panel)
- Fabric channel 1 (x4 PCI Express Gen 2, star backplane)
- Fabric channel 2 (x4 PCI Express Gen 2, dual star or full-mesh backplane)
- Fabric channels 3 to 13 (x1 Aurora or other communications standard, full-mesh backplane)
- Base channel 1 (Fast Ethernet with IEEE-1588-V2 support, star backplane)
- Base channel 2 (Fast Ethernet with IEEE-1588-V2 support, dual star or full-mesh backplane)
- Timing and synchronization (backplane MLVDS signals and Base channels)
- IPMC (CoreIPM OPMA2368 SODIMM module)
- Redundancy ready

AXIe

- Instrument module
- Single front slot (IO on the front panel)
- Fabric channel 1 (x4 PCI Express Gen 2)
- Fabric channel 2 (x4 PCI Express Gen 2)
- Base channel 1 (Fast Ethernet with IEEE-1588-V2 support)
- Timing and synchronization (backplane signals and Base channels)
- IPMC (CoreIPM OPMA2368 SODIMM module)

Processing power

- Xilinx Virtex 6 FPGA: XC6VLX240T, XC6VLX365T, XC6VSX315T or XC6VSX475T (XC6VLX365T as default)

Memory

- Up to 8 GB of DDR3 DRAM SODIMM (2 GBytes as default)
- Up to 2 GBytes of FLASH (CompactFLASH card)

IO modules

- Up to 24 modules (vertical and horizontal orientations)
- Two channels ADC module (vertical orientation)
- Two channels DAC module (vertical orientation)
- Other module options by request

ADC module, 1-2 MSPS, 18 bit with dual ADC	DAC module with dual DAC
	

IO interface

- Up to 48 channels (front or rear panel). E. g. galvanic isolated analogue inputs, galvanic isolated analogue outputs or a combination of both. Up to 24 optical multi-gigabit SFP interfaces (rear panel), etc
- Up to 12 digital FPGA 2.5 V signals (rear panel) and up to 12 digital FPGA 1.5V signals (front panel)
- One front panel SFP full-duplex multi-gigabit port (Aurora or other communication standard)
- Front panel JTAG connector for local board diagnostics
- Other module options by request

Analog inputs

- Up to 48 differential inputs (front or rear panel)
- Dynamic range: -10V to +10V (other configurations can be made by request)
- Resolution: 18 bits
- Sampling rate: 2 MSPS
- ENOB: 14 bits (expected)
- Adjacent channels crosstalk: 80 dB (expected)
- Impedance: 100 kΩ (other configurations can be made by request)
- Voltage isolation: 700 Vdc for 1 min (1 kV tested)
- Anti-aliasing filter: .... kHz passive low-pass .... rd order Butterworth (other configurations can be made by request)
- Programmable chopper switching frequency
- Connector: Male D-50

Analog outputs

- Up to 48 differential outputs (front or rear panel)
- Dynamic range: -10V to +10V (other configurations can be made by request)
- Resolution: 18 bits
- Sampling rate: 1 MSPS
- ENOB: 14 bits (expected)
- Adjacent channels crosstalk: 80 dB (expected)
- Output current: 20 mA
- Voltage isolation: 700 Vdc for 1 min (1 kV tested)
- Connector: Male D-50

FPGA external digital IO

- Up to 6 LVDS or up to 12 LVCMOS_1V5 (front panel)
- Up to 6 LVDS or up to 12 LVCMOS_2V5 (rear panel)
- Connector: Male D-37

Timing and Synchronization

- ATCA/AXIe backplane signals (redundant 100MHz clock and IRIG or others)
- ATCA/AXIe Base channels (IEEE1588-V2)
- FPGA external digital IO

JTAG

- FPGA + Xilinx SystemACE (XCCACE-TQ144I)
- Ethernet PHY 1 (DP83640TVV)
- Ethernet PHY 2 (DP83640TVV)
- IPMC (CoreIPM OPMA2368)
- RTM
- FTM

Firmware

- Local firmware upgrade through front panel CompactFLASH card
- Remote firmware upgrade capability through Hub blades (PCI Express/Ethernet) or Shelf manager (Ethernet)
- Schematics (.pdf) and FPGA pinout (.ucf) available for firmware development
- Synchronous Control and Data acquisition firmwares available

Device driver and Software

- Linux
- EPICS/CSS
- MARTe

User Manual

View the User Manual of this board.