Name	Degree	% Participation
Paulo Fortuna Carvalho	Fellow with Master	100%

Participation in the FPSC ITER Project

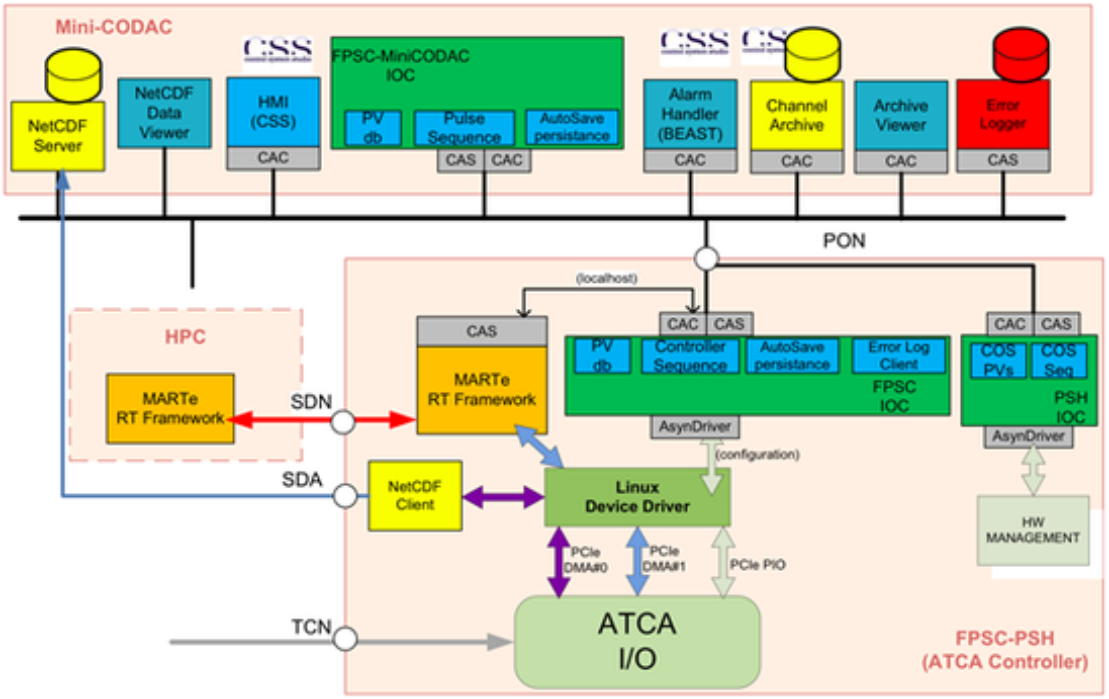


Figure 1 – ITER FPSC software system architecure

Summary and Highlights of Research Achievements

A strong effort is being done to standardize the FPSC solutions to be used in ITER. A prototype FPSC, based on ATCA form factor, was built and extensively tested against the requirements, providing crucial feedback to ITER on what are the major benefits and limitations of the tested solutions. The ATCA solution is challenging due to the lack of availability of COTS I/O solutions. However, ATCA is particularly suited as some FPSC applications (e.g., plasma vertical stabilization) need huge quantities of channels and boards with generous PCB areas are important to decrease the cost per channel.

An in-house ATCA blade for fast control and data acquisition (ATCA-IO-Processor), with IO processing capability, was developed for the FPSC to leverage the high channel density allowed by the real estate available per board for I/O channels. The high channel density makes this board a suitable solution for MIMO controllers' implementation. The card contains 48 analog channels (inputs, outputs or a combination of both) and/or digital channels (inputs, outputs or a combination of both). The architecture, compatible with the ATCA PICMG3.4 and AXIe specifications, comprises a passive RTM for I/O connectivity to ease hot-swap maintenance and simultaneously to increase cabling life cycle. The blade complies with ITER Fast Plant System Controller guidelines for rear I/O connectivity and redundancy, in order to provide high levels of reliability and availability to the Control and Data Acquisition Systems of nuclear fusion devices with

long duration plasma discharges. Simultaneously digitized data from all ADCs of the board can be filtered / decimated in a FPGA, decreasing data throughput, increasing resolution, and sent through PCI Express to multi-core processors in the ATCA shelf hub slots. Concurrently, the multi-core processors can update the board DACs in real-time. Full-duplex point-to-point communication links between all FPGAs, of peer blades inside the shelf, allow the implementation of distributed algorithms and MIMO systems. Support for several Timing and Synchronization solutions is also provided.
Another ATCA board is also under development to perform the time and synchronization functions. These boards will be part of the ITER hardware catalog for recommended items for Fast Controllers and they come with Open Source Linux device driver, user state library and EPICS Device Support. These developments diverge from the existing ATCA COTS products (that implement Ethernet on the backplane) with the implementation of PCIe on the ATCA backplane, allowing the usage of external controllers with PCIe connection for modularity. The implementation of the MARTe real-time software framework and its integration into EPICS was shown to be a powerful solution for the development of real-time controllers.
Future work will be focused on the full implementation and test of the ATCA high availability features. Such work will also address the development of radiation tolerant hardware with built in single event upset resilience. The FPSC infra-structure will also be used to the development of plasma diagnostic case studies, namely its data processing system, allowing to test algorithms and control methodologies.

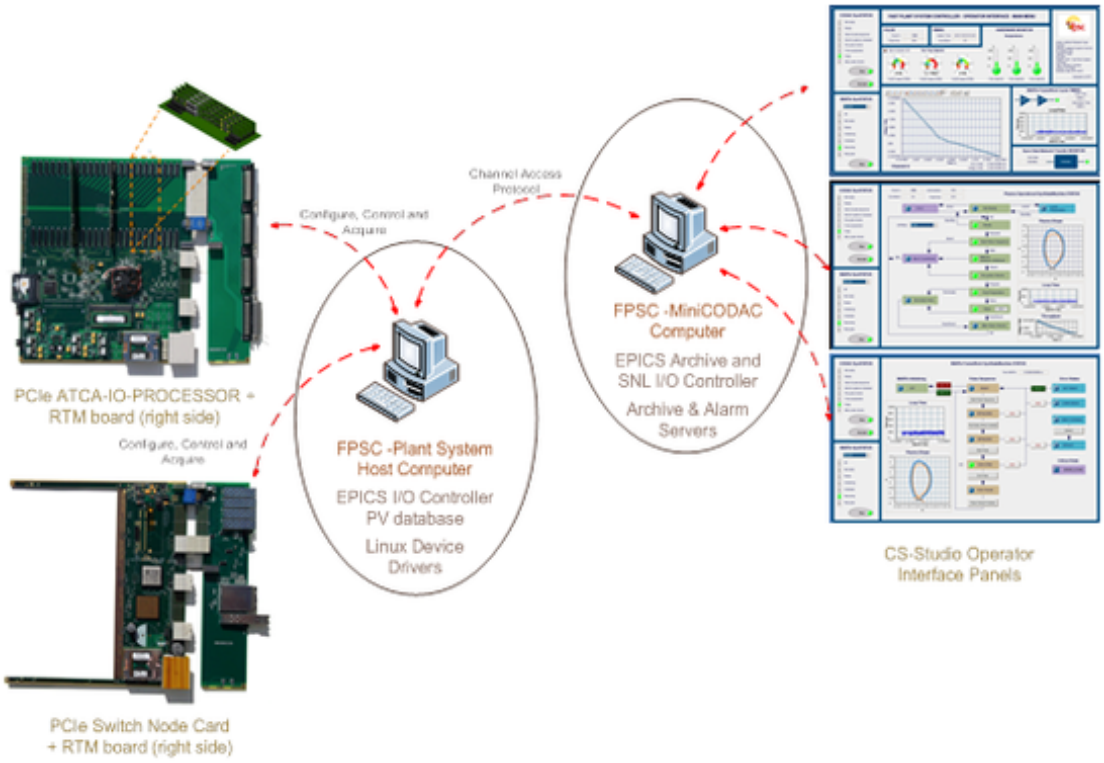


Figure 2 – EPICS software system interface

Development of an EPICS I/O controller interface for the ATCA system shelf management module.

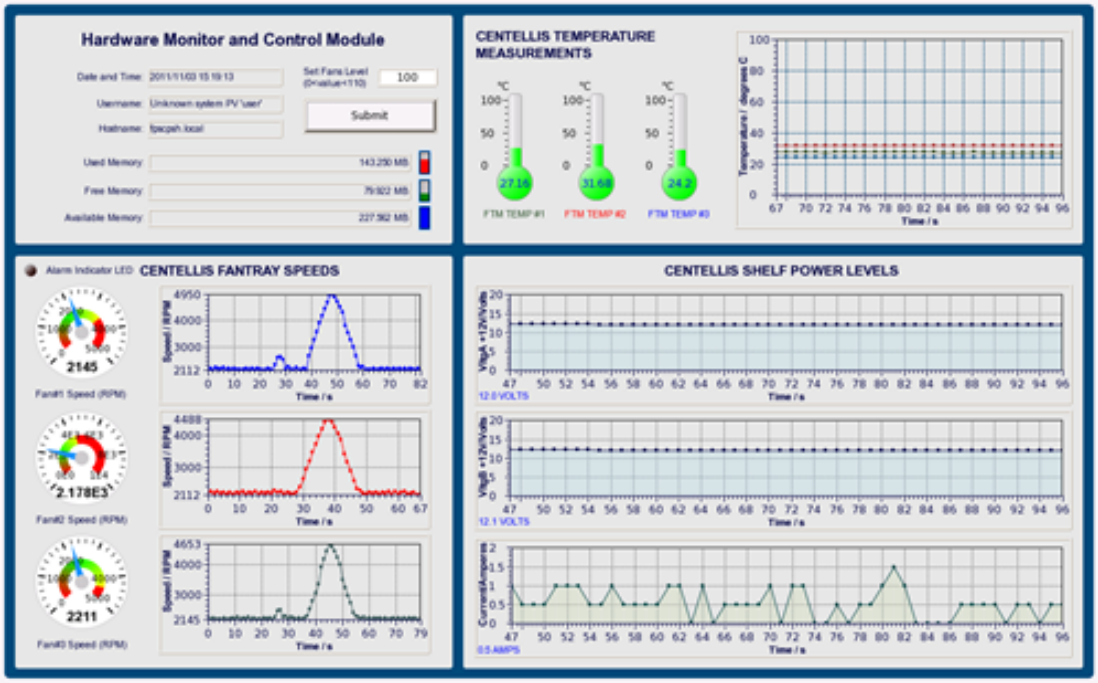
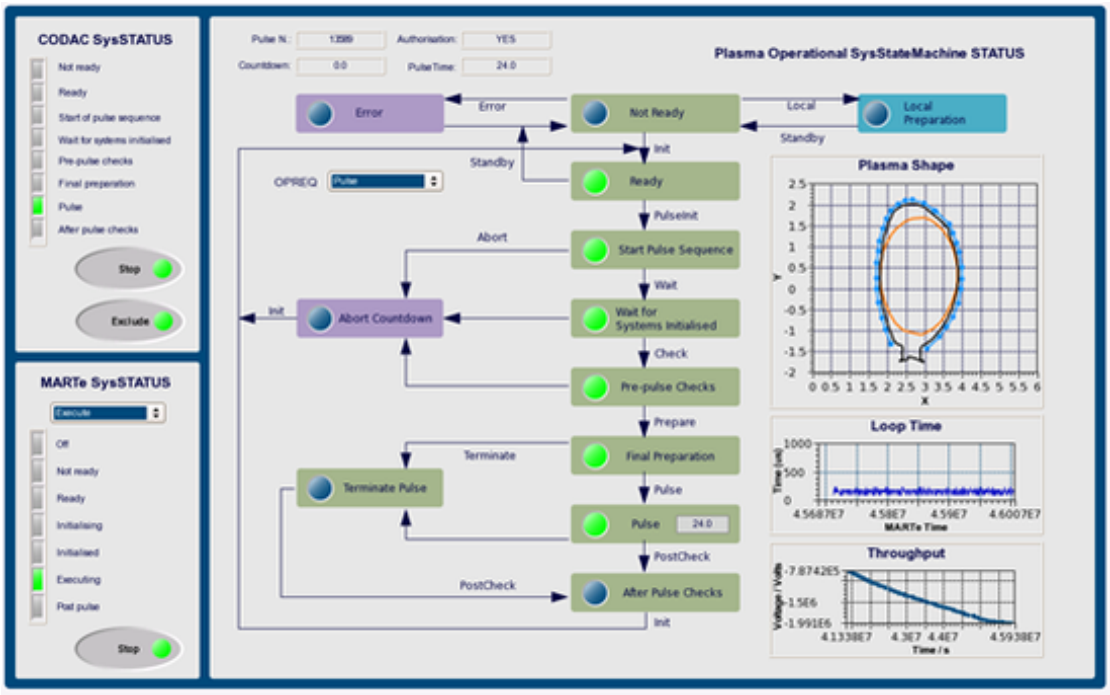
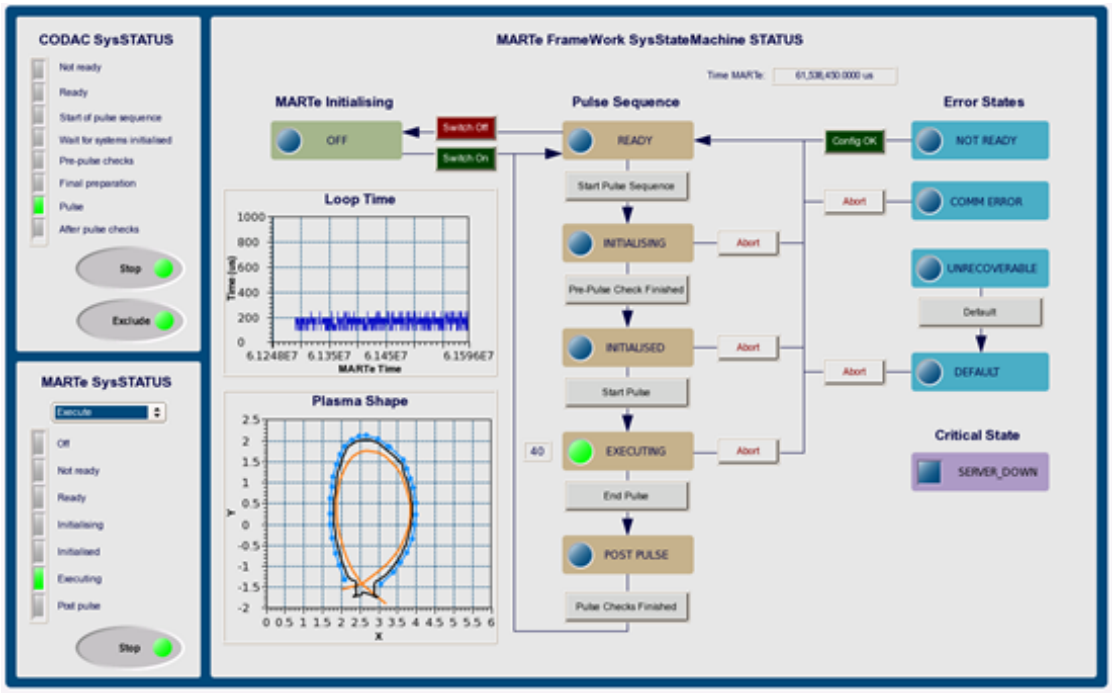


Figure 2 – HMI interface displaying the shelf management I/O controller capabilities

System State Machine interface using the SNL language implementation.



(a)



(b)

Figure 3 – CODAC System (a) and MARTe subsystem (b) state machine operation

Development and implementation of ITER FPSC System HMI based in the CS-Studio tools.

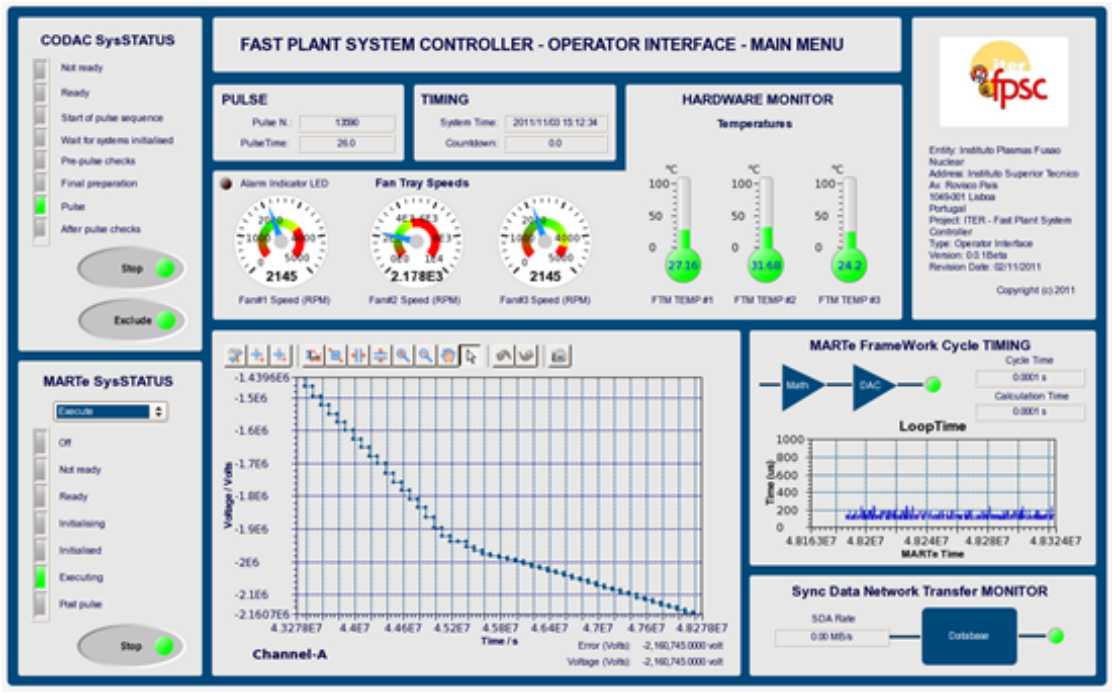


Figure 4 – ITER-FPSC System HMI Main Interface

Tests of the developed software for the FPSC Prototype

Qualitatively the performed tests results were good and are presented in the ITER Test Report documentation.

Other ITER FPSC Activities:

Co-Author and language reviewer in the ITER FPSC user guide manual documentation.

Co-Author and language reviewer in the ITER FPSC software installation guide documentation.

Co-Author and language reviewer in the ITER FPSC test report documentation.

BEAST (Alarm Handler) and BEAUTY (Archive Engine) Implementation.

IPFN and ITER SVN software packages deployment.

A. Publications

Papers in International Refereed Scientific Journals

Author(s) **P. Carvalho**, A. Duarte, T. Pereira, B. Carvalho, J. Sousa, H. Fernandes, C. Correia, B. Gonçalves, C. Varandas
Paper title EPICS IOC module development and implementation for the ISTTOK machine subsystem operation and control
Journal name Fusion Engineering and Design
Volume, page 86, 1085
Year 2011

B. Publications and Contributions in Conferences and Workshops

Oral Contributions

Conference 2011 IEEE Nuclear Science Symposium and Medical Imaging conference

Start-end date 23-29 October 2011
Location Valencia, Spain
Author(s) B. Gonçalves, J. Sousa, B.B. Carvalho, .A. Batista, A. Neto, B. Santos, A. Duarte, D.F.Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, M. Ruiz, J. Vega, R. Castro, J.M. López, N. Utzel, P. Makijarvi
Talk title ITER fast plant system controller prototype based on ATCA Platform

Conference 5th Workshop on ATCA and MicroTCA for Physics, 2011 IEEE Nuclear Science Symposium and Medical Imaging conference
Start-end date 23-29 October 2011
Location Valencia, Spain
Author(s) B. Gonçalves, J. Sousa, B.B. Carvalho, .A. Batista, A. Neto, B. Santos, A. Duarte, D.F.Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**
Talk title ATCA Developments for Fusion Fast Plasma Control Systems

Conference 8th IAEA Technical Meeting on Control, Data Acquisition, and Remote Participation for Fusion Research
Start-end date 20-24 June 2011
Location San Francisco, California, United States of America
Author(s) B. Gonçalves, J. Sousa, B.B. Carvalho, .A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, M. Ruiz, J. Vega, R. Castro, J.M. López, N. Utzel, P. Makijarvi
Talk title ITER fast plant system controller prototype based on ATCA Platform

C. Other Publications and Outputs

Technical reports

B. Gonçalves, J. Sousa, B.B. Carvalho, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, M. Ruiz, J. Vega, R. Castro, J.M. López, N. Utzel, P. Makijarvi, C. Leong, V. Bexiga, I.C.Teixeira, J.P.Teixeira, A. Barbalace, P. Lousã, J. Godinho, P. Mota, "ATCA FPSC Test Report" (November 2011)

B. Gonçalves, J. Sousa, B.B. Carvalho, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, M. Ruiz, J. Vega, R. Castro, J.M. López, N. Utzel, P. Makijarvi, C. Leong, V. Bexiga, I.C.Teixeira, J.P.Teixeira, A. Barbalace, P. Lousã, J. Godinho, P. Mota, "ATCA FPSC Test Plan" (November 2011)

B. Gonçalves, J. Sousa, B.B. Carvalho, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, M. Ruiz, J. Vega, R. Castro, J.M. López, N. Utzel, P. Makijarvi, C. Leong, V. Bexiga, I.C.Teixeira, J.P.Teixeira, A. Barbalace, P. Lousã, J. Godinho, P. Mota, "ITER FPSC Engineering Design" (September 2011)

B. Gonçalves, J. Sousa, B.B. Carvalho, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, M. Ruiz, J. Vega, R. Castro, J.M. López, N. Utzel, P. Makijarvi, C. Leong, V. Bexiga, I.C.Teixeira, J.P.Teixeira, A. Barbalace, P. Lousã, J. Godinho, P. Mota, "ITER FPSC User Manual" (November 2011)

M. Ruiz, J. Vega, R. Castro, J.M. López, B. Gonçalves, J. Sousa, B.B. Carvalho, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, N. Utzel, P. Makijarvi, "ITER FPSC PXIe Engineering Design" (September 2011)

A. Barbalace , B.B. Carvalho, B. Gonçalves, J. Sousa, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, "MARTe to EPICS Process Variables Interface" (October 2011)

Laboratorial Prototypes

B. Gonçalves, J. Sousa, B.B. Carvalho, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, M. Ruiz, J. Vega, R. Castro, J.M. López, N. Utzel, P. Makijarvi, C. Leong, V. Bexiga, I.C.Teixeira, J.P.Teixeira, A. Barbalace, P. Lousã, J. Godinho, P. Mota, "ITER Prototype Fast Plant System Controller"

M. Correia, B. Gonçalves, J. Sousa, B.B. Carvalho, A. Batista, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, A. P. Rodrigues, **P.F. Carvalho,** J. Fortunato, P. J. Carvalho, "ATCA PCIe switch"

A. Batista, B. Gonçalves, J. Sousa, B.B. Carvalho, A. Neto, B. Santos, A. Duarte, D. Valcárcel, D. Alves, M. Correia, A. P. Rodrigues, **P.F. Carvalho**, J. Fortunato, P. J. Carvalho, C. Leong, V. Bexiga, I.C.Teixeira, J.P.Teixeira, P. Lousã, J. Godinho, P. Mota, "ATCA IO Processor"

Computational and Numerical Codes

B.Santos, **P.F. Carvalho,** "MARTe Framework State Machine Panel" for EPICS CSS

B.Santos, **P.F. Carvalho,** "Synchronous Data Network Interface Panel" for EPICS CSS

B.Santos, **P.F. Carvalho,** "Data Archiving Statistics Panel" for EPICS CSS

B.Santos, **P.F. Carvalho,** "Acquisition Channels Configuration Panel" for EPICS CSS

P.F. Carvalho, B.Santos, "CODAC System State Machine" for EPICS CSS

P.F. Carvalho, B.Santos, "Memory and Processor Usage Statistics Monitoring Panel" for EPICS CSS

P.F. Carvalho, B.Santos, "Main Application Control and Monitoring Panel" for EPICS CSS

P.F. Carvalho, B.Santos, "Analogue to Digital Converter Monitoring Panel" for EPICS CSS

P.F. Carvalho, B.Santos, "Digital to Analogue Converter Monitoring Panel" for EPICS CSS

P.F. Carvalho, B.Santos, "Hardware Management Monitoring and Control Panel" for EPICS CSS

P.F. Carvalho, "devInterfaceShm-support" for EPICS IOC

P.F. Carvalho, "devInterfaceMach-support" for EPICS IOC