

TOC

1st Progress Meeting report (13th December 2011): 2

2nd Progress Meeting report (10th January 2012): 2

3rd Progress Meeting report (9th February 2012):..... 3

4th Progress Meeting report (7th March 2012):..... 3

5th Progress Meeting report (13th April 2012): 4

6th Progress Meeting report (11th May 2012):..... 4

7th Progress Meeting report (22nd June 2012): 5

Other pages:**1st Progress Meeting report (13th December 2011):**

- Board test plan in development (see respective section for details);
- Board production plan in development (see respective section for details);
- Board engineering design in development (see respective section for details);
- Firmware validated for path one and two;
- PCI express generation 2 validated;
- RTM modifications in standby until all analog IO channels are tested;
- Board tests to be done listed into the **To test** section;
- Searching in progress for a new PCB design company to make changes in order to improve the ATCA-IO-PROCESSOR prototype PCB;

2nd Progress Meeting report (10th January 2012):**Hardware:**

- Board test plan first draft ready;
- Board production plan first draft ready;
- Board engineering design first draft ready;
- Hardware engineering files and hardware production files to be stored on ITER SVN, folder structure created.

Firmware:

- Improving the stability on the continuous acquisition data streaming (DMA channel #2)

Software:

- Luca Boncagni finished his developing and tuning the MARTE system to receive RT data (report still to be finished)
- Progressing on device driver development to handle DMA channel #2

Next month**Hardware:**

- Board production (4 units) in progress;
- Hardware engineering files and hardware production files to be stored on ITER SVN, files upload in progress;
- RTM modifications in progress;
- Board tests to be done listed into the **To test** section;
- Searching in progress for a new PCB design company to make changes in order to improve the ATCA-IO-PROCESSOR prototype PCB.

Firmware:

- Integration of IPMC module with geographical address of ATCA boards on system
- Implementation of fast data transfer (DMA channel #3)

Software:

- Progressing on device driver development to handle DMA channel #2 and #3
- device Support modules to EPICS

3rd Progress Meeting report (9th February 2012):

Hardware:

- Majority of hardware engineering files and hardware production files uploaded to SVN;
- Board production in progress, but with 3 weeks delay due to components lead time changes;
- RTM modifications done, board assembled and ready to be tested;
- AXIE synchronization signals fully tested.

Firmware:

Software:

Next month

Hardware:

- Test details to be added to the test plan document;
- Board production in progress;
- FPGA and IPMC hardware engineering files and hardware production files to be stored on ITER SVN;
- Board tests to be done listed into the **To test** section;
- Searching in progress for a new PCB design company to make changes in order to improve the ATCA-IO-PROCESSOR prototype PCB.

Firmware:

Software:

4th Progress Meeting report (7th March 2012):

Hardware:

- **All hardware engineering and production files uploaded to SVN, except IPMC software and FPGA firmware (binary and source files);**
- **Board production in progress, but with 6 weeks delay due to recent IST administrative problems;**
- **RTM modifications done, board assembled and ready to be tested;**
- **More tests and test details added to the test plan document;**

Firmware:

Software:

Next month

Hardware:

- Board production in progress;
- FPGA and IPMC hardware engineering files and hardware production files to be stored on ITER SVN;
- Board tests to be done listed into the To test section;
- Searching in progress for a new PCB design company to make changes in order to improve the ATCA-IO-PROCESSOR prototype PCB.

Firmware:

Software:

5th Progress Meeting report (13th April 2012):

Hardware:

- 3 Boards produced and tests for validation started.

Firmware:

- Final version ready.

Software:

Next month

Hardware:

- FPGA and IPMC hardware engineering files and hardware production files to be stored on ITER SVN (binary and source files);
- Boards validation;
- Searching in progress for a new PCB design company to make changes in order to improve the ATCA-IO-PROCESSOR prototype PCB.

Firmware:

- Final version validation;

Software:

6th Progress Meeting report (11th May 2012):

Hardware:

- ~30% of ADC modules failed (soldering problems).

Firmware:

- **Final version validation in progress.**

Software:

Next month

Hardware:

- **Failed ADC modules validation;**
- **2 Boards to be sent ASAP;**
- **FPGA and IPMC hardware engineering files and hardware production files to be stored on ITER SVN (binary and source files);**
- **Searching in progress for a new PCB design company to make changes in order to improve the ATCA-IO-PROCESSOR prototype PCB.**

Firmware:

- **Final version validation;**

Software:

7th Progress Meeting report (22nd June 2012):

Hardware:

- **One full populated (40 ADC's and 8 DAC's) ATCA-IO-PROCESSOR module sent (June 21);**
- **Patch panel and test cables sent (June 21);**
- **One PCIe host interface card and a 3 meters PCIe cable sent (June 21).**

Firmware:

- **Final version with RTE CA fully validated.**

Software:

- **RPM available with Linux device driver, command line applications and a CSS/EPICS GUI hardware test program.**

Next month

Hardware:

- Second ATCA-IO-PROCESSOR board to be sent;
- Test Plan adjustments if needed;
- FPGA and IPMC hardware engineering files and hardware production files to be stored on ITER SVN (binary and source files);
- Searching in progress for a new PCB design company to make changes in order to improve the ATCA-IO-PROCESSOR prototype PCB.

Firmware:

- Final version DDR3 validation;

Software: