- Tracks width and differential pairs spacing in order to achieve a thinner PCB;
- Galvanic isolation tracks spacing;
- J2 Footprint;
- J59 Footprint;
- Keepout keying K1;
- Test points silk screen;
- References backannotation;
- Solder mask U51, U55 and U58;
- Terminations position;
- Decoupling capacitors position;
- FTM connector's replacement;
- RTM mechanical thickness;
- Increase space for the fan header;
- Handle switch position;
- Pin 1 position U20 and U21 (silk screen);
- FPGA I2C voltage translator - enable connected to an IPMC output or to the payload enable;
- IPMC ICs on the board;
- USB port;
- IO modules I2C bus A, B and C correction;
- Schematic corrections.