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Project

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Project Objective

•Adaptation and extension of the Fast Plant System Data Acquisition Prototypes (ITER_D_4HVBLJ) on 11/07/2011
•Goals
–Transform some of the previous delivered product “prototypes” into an ITER standard high quality products
•ATCA PCIeswitch Card – more specifically the RTM PCIeHost Interface,
•ATCA ADC module with the capability to operate either in chopper or in normal mode,
•ATCA shelf with full-mesh interconnection,
•MARTeframework integration preparation in CODAC Core System. The decision of integrating MARTein CODAC standard solutions is not acted for now. This step is a prerequisite for this decision,
•FlexRIOEPICS ASYN device support for CODAC Core System V3

Project specifications here
The proposal presented to ITER can be found here

Project Approach
•Operating Environment
–The products will operate on Red Hat Enterprise Linux 64-bits platform version 6
–For real time requirements, a tuning on Red Hat MRG extension will be required.
–The software environment and samples will be developed using Core System V2.1 distribution
•3.0.beta?

•Design and Implementation Constraints
–The dependency between the products will be minimal in order to use each product in many different configurations.
–For instance the software support of I/O modules should not rely exclusively on the MARTemodule which is only one specific use case.
–Same remark applies for the FlexRIOEPICS ASYN support device that should not be dependant of any archive or communication system.

•User Documentation

–Final engineering and design documents will be delivered for each product as well as the installationand user manuals. For existing products (MARTe), current material could be referenced and the provided documentation could only focus on CODAC integration and usage.
–The source code of each product will be organised according to CODAC standard file structure [IDM:33T8LW] and will be registered in CODAC SVN repository.
–The project will be built and managed using the mvncommands: mvncompile, mvnrun, mvnstop and mvnpackage in order to produce RPM packages and ease the deployment process

•Test Plan & Samples
–A test plan will be produced for each product detailing the different scenarios with the expected results.
–Sampleswill be produced to demonstrate the main functionalities of the product
–A monitoring screen based on CSS BOY and EPICS will be developed allowing user interaction on an EPICS IOC sample.
–The interface with the alarm server and the archive engine will also be demonstrated using CSS tools.
–The user will be allowed to change EPICS standard thresholds such as noise reduction, monitor and archive dead bands

•Assumptions and Dependencies
–CODAC will propose a standardisation of FPGA Application Register Table and an abstract model for FPGA Asyndevice support which will be provided to implement FlexRIOdriver.
–Open licensing model will be established for the products allowing all vendors to adhere and access blueprints and code according to the EURATOM licensing.

Deliverables and Due Dates

Milestone and Bidder Deliverables	Dates (weeks)	Location, Action and ITER-IO Deliverables
Kick-off meeting	T0 18/ 11/ 2011	Meeting held at ITER IO premises. Minutes of Meeting.
Delivery of the final Engineering Design Document	T0+2 weeks	These documents shall be delivered electronically.
Review	T0+4 weeks	These documents shall be commented by ITER IO. The bidder shall incorporate comments in the next version. Review Report.
Delivery of ICD and Test Plan Delivery of Production Plan (unit cost estimation)	T0+5 weeks	These documents shall be delivered electronically.

Review	T0+7 weeks	These documents shall be commented by ITER IO. The bidder shall incorporate comments in the next version. Review Report.
Delivery of the products with their engineering design documents, test plan and samples	T0+12 weeks	The products will be shipped to ITER IO. The code source and samples will be delivered in SVN. These documents shall be delivered electronically.
Improvement of the product quality	T0+30 weeks	Iterative process. Integration of IO comments and submitted bugs. Monthly Bugs Report.
Delivery of all final documentation and samples for the products	T0+32 weeks	Finalisation. End of task

Acceptance Criteria

•Each product will be manufactured in small quantity early in the project – including hardware and software (Linux driver, EPICS device support, samples)

•3 x ATCA PCIeswitch Cards,
•2 x ATCA ADC modules,
•1 x ATCA shelf with full-mesh interconnection specification,
•1 x MARTepackage,
•1 x FlexRIOEPICS ASYN package.
•Each product will be tested by IO and other labs
according to the delivered test plan
•This is an iterative process in order to improve the product quality

Project Management
•Meetings
–Progress reports shall be submitted by IST every month
–Minutes of meetings and review reports, including action item lists, will be written by ITER- IO
•Issue Management
–SharePoint site and actions tracking
–Bugzilla
•Change Management
–SVNcontract>> https://svnpub.iter.org/codac/iter/codac/dev/units/

•Risk Management
–None

Internal Organization