Issue	Question	Answer
1	What is voltage rating of the Galvanic Isolation of RTM_IO_X? · Between tracks on the same pair. · Between pairs on the same “Double-pair” (Pair-AB) · Between “Double pairs”	 no galvanic isolation each pair shielded with groundShielding for RTM File:/C:\Users\Alvaro\AppData\Local\Temp\msc Shielding for pair A and B channel 1 (700Vdc) File:/C:\Users\Alvaro\AppData\Local\Temp\msc Shielding for pair A and B channel 2 [OK]
1a	**Shielding:**Shielding is possible on board traces, BUT will NOT EXTEND to the connectors area. Is this acceptable?	Yes [OK]
1b	**Galvanic Isolation (1):(Example) On** 6469169-1 connector the pin-to-pin distance is 2.5mm (between different “double pairs”). Assuming a 1mm “pad” diameter (as specified in connector data sheet) leaves 1.5 mm for passing ONE pair of signals (not shielded-see 1a), BUT that should have 700Vdc Isolation. Is this acceptable? (Note: Assumed tracks are routed in internal layers) Other connectors may have similar problems. Minimum clearance trough FR4 should be stated.	Yes please ignore the 700Vdc spec and try to do t [OK]
1c	**Galvanic Isolation (2):**What is the minimum clearance on free-air for 700Vdc? (this directly relates with 8 and 8a)	Please ignore the 700Vdc spec and route galvanic maximum distance between them [OK]

2	What is the voltage/current rating of each RTM_IO_X? (Or what is the minimum required track width?)	Analogue differential pairs up to +/- 50V and trac width for the required impedance, see below [OK]
2a	**Voltage and current rating**: Assuming 100V maximum voltage across a 100 ohm impedance, gives 1A current rating. For internal layers (with 2oz) this gives trace widths greater than **390µm**. 100Ω differential impedance is not achievable (requires about 1mm dielectric thickness). Change specifications for achievable conditions. (see 3a)	Yes decrease the 100V maximum voltage [OK]
3	An RTM_IO_X pair is a differential pair? If yes, what should be their impedance (and other relevant characteristics)?	100 Ohms differential pair impedance with best m [OK]
3a	Assuming a 100Ω target **<u>differential impedance</u>** (ε_r=4.2; Trace width= 150µm; Fr4Thick=300µm (symmetric); Separation=215µm; 2oz): · Simulator #1 (http://www.skottanselektronik.com/): Z_{diff}=100Ω / Z_0=60 Ω · Simulator #2 Polar Instruments: Z_{diff}=88 Ω (No Z_0 calculated) What should be the actual values? (Please check 2a for voltage/current ratings)	100 Ohms +/- 15 Ohms (Request validation of final Impedance when avai Considering the current settings for stacking and 91.71 Ω (calculated by Polar (does not include side impedance). Settings(µm): H_1=180; H_2=200; T_{Thick}=17.5 (1/2 oz
4	Can a Pair-AB share the shielding Ground? (If possible detail shielding requirements: side track width, adjacent layer oversize track, required stitching vias, etc.)?	Yes [they can share Ground]. Probably no stitchin pairs only for RTM_DIO_X [OK]
5	RTM is considered a "Backplane" for z-pack-2 Definitions? (Should backplane pinout be considered?)	yes is a backplane and the footprint has a backpla [OK]
6	In ARTM power supply connector is in the TOP. This is not in the agreement of the requested layout drawing and conflicts with the pinout which may	The power connector is to be below the z-pack-2 RTM_IO_X pairs with power and RTM-DIO-X pairs

	require digital signals crossing IO signals. Is this to be maintained? Request for connector positioning coordinates (See 13 for important information).	To be defined(Issue clarified)[OK]
6a	Required the following information: 1. Form factor (or changes relative to standard) 2. Definition of positioning coordinates for power and data connectors (data connector assumed "packed").	To be defined 1 – Still open. The form factor is proprietary and specifications. [OK] 2- [OK]
7	Requested EEPROM is assumed to be connected with the specified ARTM I2C power pinout connector.	Yes SDA, SDL signals and the power supply is the [OK]
8	On the D-Sub50 connector each Pair-AB should be assigned ONE, TWO or Three Ground pins? This is key for the definition of isolation.	Minimum one, but the pinout, if possible, with cr B pairs
8a	Comment: This question was not intended to refer to crosstalk, but to Galvanic Isolation. IF Clearance (on connector – trough air) can be considered only pin-to-pin then three grounds can be used to improve crosstalk. IF clearance requires more than pin-to-pin spacing (AND intermediate floating pin is acceptable) then less ground signals must be used.	Pin-to-pin (2.54mm)
9	An RTM_DIO_X pair is a differential pair? If yes, what should be their impedance (and other relevant characteristics)?	100 Ohms differential pair impedance with best m Shielding for RTM_DIO pairs File:/C:\Users\Alvaro\AppData\Local\Temp\msc (Request validation of final Impedance when avai
9a	See 3a (no voltage rating concerns).	[OK]
10	What should be the name of the board?	ATCA-IO-PROCESSOR_RTM [OK]

11	What is the deadline?	Assembled early September (Waiting for holiday scheduling)
12	Confirm that RTM connector is **2065769-1** (http://www.te.com/catalog/pn/en/2065769-1?RQPN=2065769-1)	Connector to be used: 6469169-1. (http://www.te.com/catalog/pn/en/6469169-1) [OK]
13	Changing power supply connector requires changing in the RTM form factor. What is the form factor to be used? (See page 24 of PICMG 3.8 RC1.0f)	SEE 6a [OK]
14	Verify if the following DSub connectors can be used: · Dsub-37: http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=ADF37A-KG-TAXB3-R-ND · Dsub-50: http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=A31816-ND	Dsub-37 yes Dsub-50 is possibly better for galvanic isolation to files/TB_0966562x81x_BL01_R29733.pdf(suggesti File:/C:\Users\Alvaro\AppData\Local\Temp\msc [OK]
14a	Validate the following components: · DSub-37: Digikey (ADS37A-KG-TASB5-R-ND) – Assmann Electronics (ADS37A-KG-TASB5-R). **IMPORTANT**: **Male**connectors WITH 2.84mm Row Pitch ARE NOT on stock on main suppliers. http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=ADS37A-KG-TASB5-R-ND– Please advise on solution. · DSub-50: Farnell (1200491) – Harting (09 66 562 7811) - http://pt.farnell.com/harting/09-66-562-7811/plug-d-pcb-r-a-50way/dp/1200491	DSub-50 ok[OK] DSub-37 please use the more common 2.76mm by DSub-37 Replaced: see 14b [OK]

Gender	Male connector, right angled
Termination	turned solder pins

	Shell	tinned metal shell with dimples
	Number of contacts	50
	Row pitch	Row separation 2.54 mm
	Board fixing	with snap-in-clips
	Grounding	with grounding board locks
	Flange	M 3
	Performance level	Performance level 3
	Material	PBTP
	Termination	turned solder pins
14b	Validate following: · DSub-37: Farnel (1097067) – Harting (9 65 462 6812). http://pt.farnell.com/harting/09-65-462-6812/plug-d-pcb-r-a-37way/dp/1097067(250 mating cycles)	yes [OK]
15	Changes in ARTM standard have changed the power connector pin assignment. What should be the procedure?	Pinout: File:/C:\Users\Alvaro\AppData\Local\Temp\msc [OK]
16	**6469169-1 PCB Design issue**: On "*Application Specification 114-13059*" (ENG_SS_114-13059_K), Figure 3, seems that the Diameter of PCB holes is 0.05mm (which is clearly too small). In figure 4 (of the	Very strange the hole diameter Please use oval pads 1mm major dimension Au finish on all board

	document) is presented the detailed specifications of the PCB Hole. The following questions/comments: · Assume that Figure 4 has the correct values. · In Allegro what should be the dimensions (considering the design)? o Drill Diameter: 0.675-0.725 o Top/Bottom: 1mm o Inner? o What finish should be used (For HM_Zd Au finish is not specified).	The hole dimensioning was assumed to be correct Specification – figure 4).
16a	Since connector is to be soldered (instead of seated), is required to increase the size of holes in the PCB footprint. Current drill is 0,7mm (in-line with specified). What should be the oversize hole?	Holes have been set with the same characteristics connector is to be soldered. [OK]
17	Check how many and type of signals implemented in the board. 1. In DSub-37 pin assignment appear two sets of eight pairs (**total of 16 pairs**) named a. CH ? src: Assumed Channel Source acronym. b. CH ? +/-: Assumed Channel Sink acronym. 2. In Schematic template sent appear **SIX** pairs named RTM_DIO_?_P/N: Assumed Input/output digital signals. 3. Each DSub-50 connectors is said to have SIX pairs of Analogue signals (**total of 24 pairs**). This is in line with schematic template.	1a) src (screen) is the respective channel ground 2a) 8 differential channels [OK] 2) Connect the six pairs to channel 1 up to 6 of DS Unconnected) 3) Each DSub-50 has 16 pairs (channels) the total
17a	Undefined/incorrect connection between DSub-37 and RTM connector. In template schematic ALL grounds in the RTM connector (refereeing to digital signals) are connected to GND. If scr is a by-channel ground then they are to be splitted?	No need to split. The DSub-37 pinout is the JET pi use and is prepared to allow galvanic isolation. In galvanically isolated and share the same ground. to the common digital GND plane. [OK]

18	ARTM Standard Compliance: Despite non-compliance of board regarding (some) physical layout, does electrical and logical compliance is to be maintained? · Pull-up on ENABLE#. · Schottky diode t Ground in PS#. · Pull-ups on SDA and SCL lines of I2C. · Key alignments should be put in place.	· Pull-up on ENABLE#. No, leave unconnected · Schottky diode t Ground in PS#. yes · Pull-ups on SDA and SCL lines of I2C. No · Key alignments should be put in place. Yes [OK]
19	The EEPROM to be included (24LC014H) complies with the following: · Address: 0b000 · Write Protection: Disabled (0b0)? · Power Supply: connect to 3.3V or 3.3V_MGMT?	· Address: 0b000 [OK] · Write Protection: Disabled (0b0)? If possible [OK] · Power Supply: 3.3_MGMT [OK]
20	Please add the 2.5V and 3.3V to the DSub-37 connector pins 36 and 37 respectively. Same ground plane as DIO signals.	Implementation done [OK]
21	Confirm that PCB holes for SP7KH4M0BS0A1 are to be set to 0.8mm	Yes 0.8mm[OK]
22	Confirm that RTM key alignment components are the following: · K1: 1469374-1 (http://www.te.com/catalog/pn/en/1469374-1?RQPN=1469374-1) · K2: 1-1469372-1 (http://www.te.com/catalog/products/en?q=1-1469372-1) (Note: The footprint was changed to have five Holes.)	K1 yes[OK] K2 yes, attention shift footprint 9.8 mm to the rig connectors PCB edge (please ignore the standard is not standard... see 6a)) [OK]
23	Change top-left corner to 45º for better guide insertion.	[OK]
24	Add conformal coat on stack.	· Unable to ADD Conformal Coat on Bottom La add layers between copper and Air on bottom lay

		· Adding conformal coat on above TOP layer i added. Material is not available; it must be added what path to follow.
25	Add stitching vias on digital differential pairs.	[OK]
26	Check D-37/50 positioning.	Considering the following: 1. RTM dimensioning (as Fig.2-19) of PICMG3.0 R of PICMG 3.8, RC1.0f. 2. RTM test dimensions presented on PICMG 3.8 distance to the rear-panel. 3. The Db-37 and Db-50 Data Sheets. 4. Current position of Dsub-pin closer to PCB-ed o Db-37: 8.3mm o Db-50: 8.53mm It follows that: a) Board width (at lower area) is 68mm. b) Distance from board edge to rear panel is 4.5 c) Distance from DSub pin (closer to edge) to m This means that distance from connectors to rear · Db-37: 4.54 – (10.4-8.3)= 2.44mm · Db-50: 4.54 – (10.4-8.53)= 2.67mm Please verify is assumptions are correct.