

Historic

| Date | Version | Description | Author |
|---------------|---------|-----------------|--------|
| 16-April-2012 | 1.0 | Initial Version | ACombo |

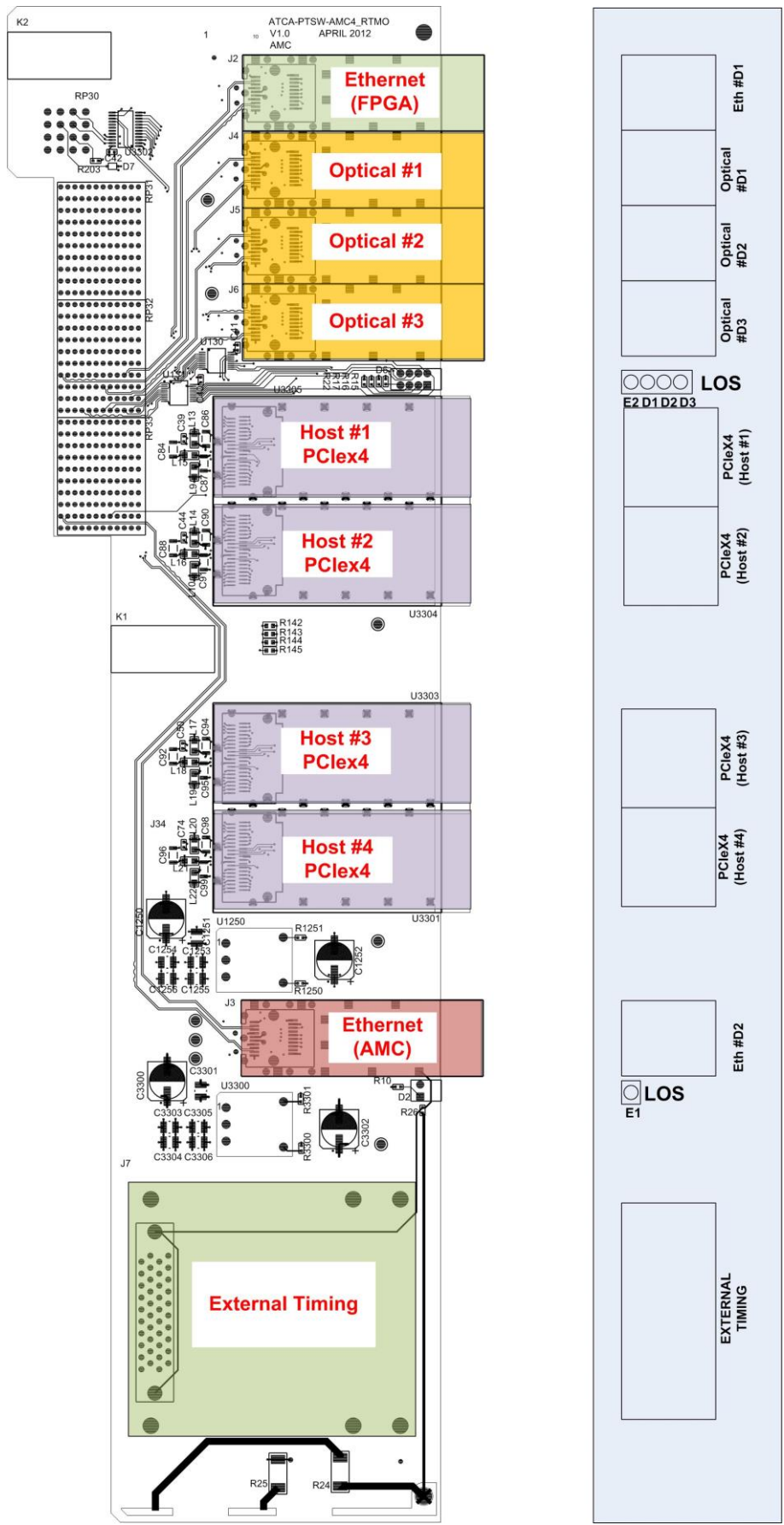
Description

The ATCA-PTSW-AMC4-RTMO is a xTCA^[1] based module that follows the specifications presented in PICMG^[2]® PhysRTM.0, Revision 1.0 Draft 0.1g that complements PICMG[®] 3.0, Revision 3.0^[3] with respect to ARTM specification.

The module acts as a passive External multiple-Host to ATCA Base carrier interface, providing the required electrical and logical connections, with status information.

The module implements the following functions:

- Four PCI Express 4 lane over fibre cable, compliant with v1.x., operating as a downstream system using ATCA Base carrier with a PCIe bay. The PCIe lanes are mapped on ATCA Base Carrier according Table 2.
- Two Gigabit Ethernet ports that are mapped on ARTM connector according Table 3.
- Three General purpose Optical interfaces^[4] using SFP (Small form-factor pluggable) connector. These ports are mapped on ARTM connector according Table 4.
- External timing and trigger features connector.
- The ARTM provides features for control and status of on-board devices that are mapped on the ARTM, according tables referenced above.



Board Infrastructure

ARTM Power Connector

This connector follows specifications of *AdvancedTCA Rear Transition Module Zone 3A*, *PICMG® 3.8, R1.0 D0.9* from 9 March 2011.

SCL_L and SDA_L of this connector implement a two-wire interface from the carrier board to the ARTM devices.

Table 1. Power/Management Connector Pin (see Table 2-1 of specification).

| Pin # | Use | Pin # | Use | Pin # | Use | Pin # | Use |
|-------|-----------|-------|------------------|-------|----------|-------|----------|
| A1 | MP | A2 | MP Rtn | A3 | PWR | A4 | PWR Rtn |
| B1 | Shelf Gnd | B2 | PS# ¹ | B3 | PWR | B4 | PWR Rtn |
| C1 | SCL_L | C2 | SDA_L | C3 | ENABLE# | C4 | Reserved |
| D1 | JTAG TCK | D2 | JTAG TDO | D3 | JTAG TDI | D4 | JTAG TMS |

ARTM Fabric Connectors Pinout (ATCA -Zone 3)

The Fabric connector follows AdvancedTCA Rear Transition Module Zone 3A, PICMG® 3.8, R1.0 D0.9xc from 3 May 2011 that points out to PICMG®3.3 Revision 3.0 AdvancedTCA® Base Specification and auxiliary documents.

The RP31 ARTM may or may not be assembled. There is no internal connection for this connector.

Table 2. PCI Express lanes mapping on the ARTM connector and corresponding Host Assignment.

| Con | Pin | Signal | Fiber Host | | Con | Pin | Signal | Fiber Host | |
|------|-----|------------|------------|---------|------|-----|------------|------------|---------|
| | | | Lane | | | | | Lane | |
| Rp33 | F1 | Port_0_Tx- | L#0 | Host #0 | Rp33 | F5 | Port_8_Tx- | L#0 | Host #2 |
| Rp33 | E1 | Port_0_Tx+ | | | Rp33 | E5 | Port_8_Tx+ | | |
| Rp33 | H1 | Port_0_Rx- | | | Rp33 | H5 | Port_8_Rx- | | |
| Rp33 | G1 | Port_0_Rx+ | | | Rp33 | G5 | Port_8_Rx+ | | |
| Rp33 | B1 | Port_1_Tx- | L#1 | | Rp33 | B5 | Port_9_Tx- | L#1 | |

| | | | | | | | |
|--------|------------|-----------------|---------|--------|-------------|---------------------------|---------|
| Rp33A1 | Port_1_Tx+ | | | Rp33A5 | Port_9_Tx+ | | |
| Rp33D1 | Port_1_Rx- | | | Rp33D5 | Port_9_Rx- | | |
| Rp33C1 | Port_1_Rx+ | | | Rp33C5 | Port_9_Rx+ | | |
| Rp33F2 | Port_2_Tx- | | | Rp33F6 | Port_10_Tx- | | |
| Rp33E2 | Port_2_Tx+ | L#2 | | Rp33E6 | Port_10_Tx+ | L#2 | |
| Rp33H2 | Port_2_Rx- | | | Rp33H6 | Port_10_Rx- | | |
| Rp33G2 | Port_2_Rx+ | | | Rp33G6 | Port_10_Rx+ | | |
| Rp33B2 | Port_3_Tx- | | | Rp33B6 | Port_11_Tx- | | |
| Rp33A2 | Port_3_Tx+ | L#3 | | Rp33A6 | Port_11_Tx+ | L#3 | |
| Rp33D2 | Port_3_Rx- | | | Rp33D6 | Port_11_Rx- | | |
| Rp33C2 | Port_3_Rx+ | | | Rp33C6 | Port_11_Rx+ | | |
| Rp33F3 | Port_4_Tx- | | | Rp33F7 | Port_12_Tx- | | |
| Rp33E3 | Port_4_Tx+ | L#0 | | Rp33E7 | Port_12_Tx+ | L#0 | |
| Rp33H3 | Port_4_Rx- | | | Rp33H7 | Port_12_Rx- | | |
| Rp33G3 | Port_4_Rx+ | | | Rp33G7 | Port_12_Rx+ | | |
| Rp33B3 | Port_5_Tx- | | | Rp33B7 | Port_13_Tx- | | |
| Rp33A3 | Port_5_Tx+ | L#1 | | Rp33A7 | Port_13_Tx+ | L#1 | |
| Rp33D3 | Port_5_Rx- | | | Rp33D7 | Port_13_Rx- | | |
| Rp33C3 | Port_5_Rx+ | | Host #1 | Rp33C7 | Port_13_Rx+ | | Host #3 |
| Rp33F4 | Port_6_Tx- | | | Rp33F8 | Port_14_Tx- | | |
| Rp33E4 | Port_6_Tx+ | L#2 | | Rp33E8 | Port_14_Tx+ | L#2 | |
| Rp33H4 | Port_6_Rx- | | | Rp33H8 | Port_14_Rx- | | |
| Rp33G4 | Port_6_Rx+ | | | Rp33G8 | Port_14_Rx+ | | |
| Rp33B4 | Port_7_Tx- | | | Rp33B8 | Port_15_Tx- | | |
| Rp33A4 | Port_7_Tx+ | L#3 | | Rp33A8 | Port_15_Tx+ | L#3 | |
| Rp33D4 | Port_7_Rx- | | | Rp33D8 | Port_15_Rx- | | |
| Rp33C4 | Port_7_Rx+ | | | Rp33C8 | Port_15_Rx+ | | |
| Rp33F9 | CPERST# | Reset All Hosts | | Rp32F9 | PRSNT# | At least One Host Present | |

| | | | | | | | |
|------|----|------------|-------------------------|------|----|------------|---|
| Rp32 | E9 | WAKE# | Interrupt from Any Host | Rp32 | H9 | PWRON | Low Power Mode (All Hosts). Set to LOW. |
| Rp33 | H9 | RTM_FCLKA- | Not Connected | Rp33 | G9 | RTM_FCLKA+ | Not Connected |

Table 3. Giga-bit Ethernet mapping (SFP Connector) on the ARTM connector.

| Con | Pin | Signal | Description | Interface |
|------|-----|----------------------|------------------------------|-----------------------|
| Rp33 | B9 | GbE_Port_0_Tx- | Gigabit Transmit Signal-pair | AMC #1 Site |
| Rp33 | A9 | GbE_Port_0_Tx+ | | |
| Rp33 | D9 | GbE_Port_0_Rx- | Gigabit Receiver Signal-pair | |
| Rp33 | C9 | GbE_Port_0_Rx+ | | |
| Rp32 | B9 | RTM_SFP_TX_DISABLE_1 | SFP Transmit Disable | |
| Rp32 | A9 | RTM_SFP_LOS_1 | SFP Loss of Signal (*) | |
| Rp32 | F7 | GbE_Port_1_Tx- | Gigabit Transmit Signal-pair | FPGA Ethernet Port #0 |
| Rp32 | E7 | GbE_Port_1_Tx+ | | |
| Rp32 | H7 | GbE_Port_1_Rx- | Gigabit Receiver Signal-pair | |
| Rp32 | G7 | GbE_Port_1_Rx+ | | |
| Rp32 | D9 | RTM_SFP_TX_DISABLE_2 | SFP Transmit Disable | |
| Rp32 | C9 | RTM_SFP_LOS_3 | SFP Loss of Signal (*) | |

(*) Depending on SFP connector used, this signal may not be used.

Table 4. Optical SFP connector mapping on the ARTM connector.

| Con | Pin | Signal | Description | Interface ⁶ |
|------|-----|----------------------|------------------------|------------------------|
| Rp32 | B7 | IO_Port_1_Tx- | Transmit Signal-pair | FPGA MGT Port #? |
| Rp32 | A7 | IO_Port_1_Tx+ | | |
| Rp32 | D7 | IO_Port_1_Rx- | Receiver Signal-pair | |
| Rp32 | C7 | IO_Port_1_Rx+ | | |
| Rp32 | F10 | RTM_SFP_TX_DISABLE_3 | SFP Transmit Disable | |
| Rp32 | E10 | RTM_SFP_LOS_3 | SFP Loss of Signal (*) | |

| | | | | |
|------|-----|----------------------|------------------------|------------------|
| Rp32 | F8 | IO _Port_2_Tx- | Transmit Signal-pair | FPGA MGT Port #? |
| Rp32 | E8 | IO _Port_2_Tx+ | | |
| Rp32 | H8 | IO _Port_2_Rx- | Receiver Signal-pair | |
| Rp32 | G8 | IO _Port_2_Rx+ | | |
| Rp32 | H10 | RTM_SFP_TX_DISABLE_4 | SFP Transmit Disable | |
| Rp32 | G10 | RTM_SFP_LOS_4 | SFP Loss of Signal (*) | |
| Rp32 | B8 | IO _Port_3_Tx- | Transmit Signal-pair | FPGA MGT Port #? |
| Rp32 | A8 | IO _Port_3_Tx+ | | |
| Rp32 | D8 | IO _Port_3_Rx- | Receiver Signal-pair | |
| Rp32 | C8 | IO _Port_3_Rx+ | | |
| Rp32 | B10 | RTM_SFP_TX_DISABLE_5 | SFP Transmit Disable | |
| Rp32 | A10 | RTM_SFP_LOS_5 | SFP Loss of Signal (*) | |

(*) Depending on SFP connector used, this signal may not be used.

Table 5. Clock, Trigger and user defined signals mapping on the ARTM connector.

| Con | Pin | Signal | Description | Interface ⁶ |
|------|-----|--------------|------------------|------------------------|
| Rp33 | F10 | RTM_CLK- | External Clock | FPGA I/O - TCLKB |
| Rp33 | E10 | RTM_CLK+ | | |
| Rp33 | H10 | RTM_AUX- | User defined | FPGA I/O - TCLKC |
| Rp33 | G10 | RTM_ AUX + | | |
| Rp33 | B10 | RTM_IRIG- | IRIG Time Code | FPGA I/O - TCLKD |
| Rp33 | A10 | RTM_ IRIG + | | |
| Rp33 | D10 | RTM_TRG- | External Trigger | FPGA I/O - TCLKCA |
| Rp33 | C10 | RTM_TRG+ | | |
| Rp32 | G9 | RTM_SIGNAL | User defined | FPGA I/O |
| Rp32 | D10 | RTM_SPAREIO- | User defined | |
| Rp32 | C10 | RTM_SPAREIO+ | | |

PCIeX4 Host Connectors

The ATCA-PTSW-AMC4-RTMOModule has four Four-Channel, pluggable, parallel, fiber-optic QSFP+ transceivers from Avago Technologies [\[6\]](#).

The PCI Express port mapping into the ARTM fabric connector is depicted in Table 2.

The transceivers can be accessed through a two-wire serial interface that is mapped on the ARTM power connector interface (see section 2.1). Since the ARTM power connector provides a single port a de-multiplexing is implemented (see section 3.1).

Details about transceiver configuration can be found in section 3.2.

Gigabit Ethernet Connectors

The RTM_Host Module has two 1000BASE-T 1.25 GBd Small Form Pluggable (SFP) electrical transceivers over Category 5 Cable. The transceivers used are ABCU-5710RZ [\[7\]](#) from Avago Technologies.

These Ethernet ports are mapped into ARTM fabric connector as depicted in Table 3.

The transceivers can be accessed through a two-wire serial interface that is mapped on the ARTM power connector interface (see section 2.1). Since the ARTM power connector provides a single port a de-multiplexing is implemented (see section 3.1).

Details about transceiver configuration can be found in section 3.3.

Gigabit Optical Connectors

The RTM_Host Module has three Short-Wavelength Pluggable (SFP) Transceivers from Finisar, capable of up to 1.25 Gb/s duplex with a 850 nm VCSEL laser transmitter.

These Gigabit Optical ports are mapped into ARTM fabric connector as depicted in Table 4.

Clock, Trigger and GPIO Connector

The RTM_Host Module includes a connector that may be used for the distribution of several clock signal and general purpose signals. The following table presents the connector pinout.

Table 6. Clock and General purpose Connector pinout (J7).

| Pin | Signal | Description |
|------------------------------------|--------------|--|
| 1 | RTM_TRG- | External Trigger |
| 3 | RTM_TRG+ | |
| 5 | RTM_IRIG- | IRIG Time Code |
| 7 | RTM_ IRIG + | |
| 9 | RTM_AUX- | User defined |
| 11 | RTM_ AUX + | |
| 13 | RTM_CLK- | External Clock |
| 15 | RTM_CLK+ | |
| 17 | RTM_SPAREIO- | User defined |
| 19 | RTM_SPAREIO+ | |
| 40 | SIGNAL | User defined |
| 2, 4, 6, 8, 10, 12, 14, 16, 18, 20 | GND | Ground |
| 22, 24 | RTM_12V | RTM 12V Power. |
| 26, 28 | RTM_3V | RTM 3.3V Power. |
| 30, 32 | 3V3 | Adjustable power supply (Default 3.3V) |
| 34, 36 | VTD25 | RTM 2.5V Power. |

Configuration Settings and Status

Configurations of ATCA-PTSW-AMC4-RTM0module are limited to transmitter/receiver connector/chipsets where protocol and/or physical operation condition may be changed. In addition some features may be used to identify installed infrastructure. The configuration is performed through the Power and Management plug on Zone 3 (see Table 1).

Status will be available through Led's on rear panel and on Zone 3 Data Connectors as presented on .

General Configuration

The ARTM configuration uses I2C protocol at address **0x70**. The ARTM has two internal devices that may require configuration, which are the two Gigabit Ethernet ports. The access and configuration must be supported by the ATCA Host Board.

Table 7 presents the mapping for the I2C switch (PC9548A from NXP Semiconductors®) with the indication of Control bit register (Figure 2) that enables each port. For detailed information regarding I2C switch PCA9548A data sheet [\[8\]](#) must be consulted.

Table 7. Mapping of ARTM I2C devices into PCA9548A ports.

| PCA9548A Port | Control Register bit | ARTM Device |
|---------------|----------------------|---|
| Port #0 | Bit-0 | PCleX4 Optical Host #1 |
| Port #1 | Bit-1 | PCleX4 Optical Host #2 |
| Port #2 | Bit-2 | PCleX4 Optical Host #3 |
| Port #3 | Bit-3 | PCleX4 Optical Host #4 |
| Port #4 | Bit-4 | Ethernet Port (Connected to Carrier FPGA) |
| Port #5 | Bit-5 | Ethernet Port (Connected to Carrier AMC Bay #0) |
| Port #6 | Bit-6 | Not Used |
| Port #7 | Bit-7 | Not Used |

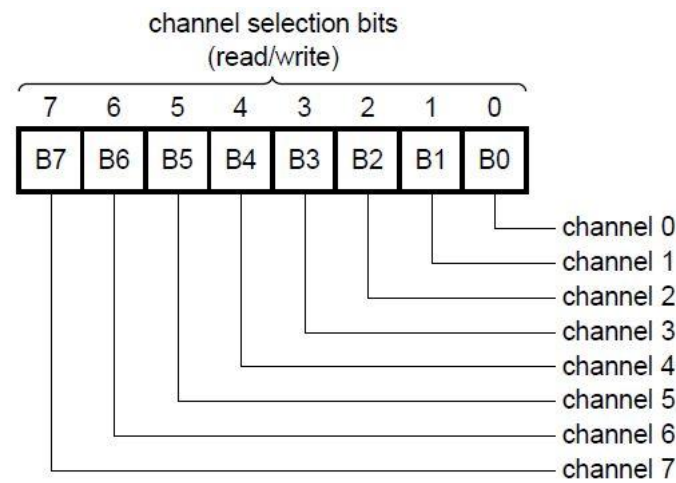


Figure 2. PC9548A Control bit Register.

3.2 PCIe Optical PHY Configuration

The AFBR-79EQDZ PHY has single address, multiple page memory map architecture accessed through I2C on the base address **0xA0**.

The component has a 256-byte address range (starting in 0xA0). The lower 128-bytes are directly accessed. The higher 128-bytes access the selected page (Figure 3). For further details see AFBR-79EQDZ data sheet[9].

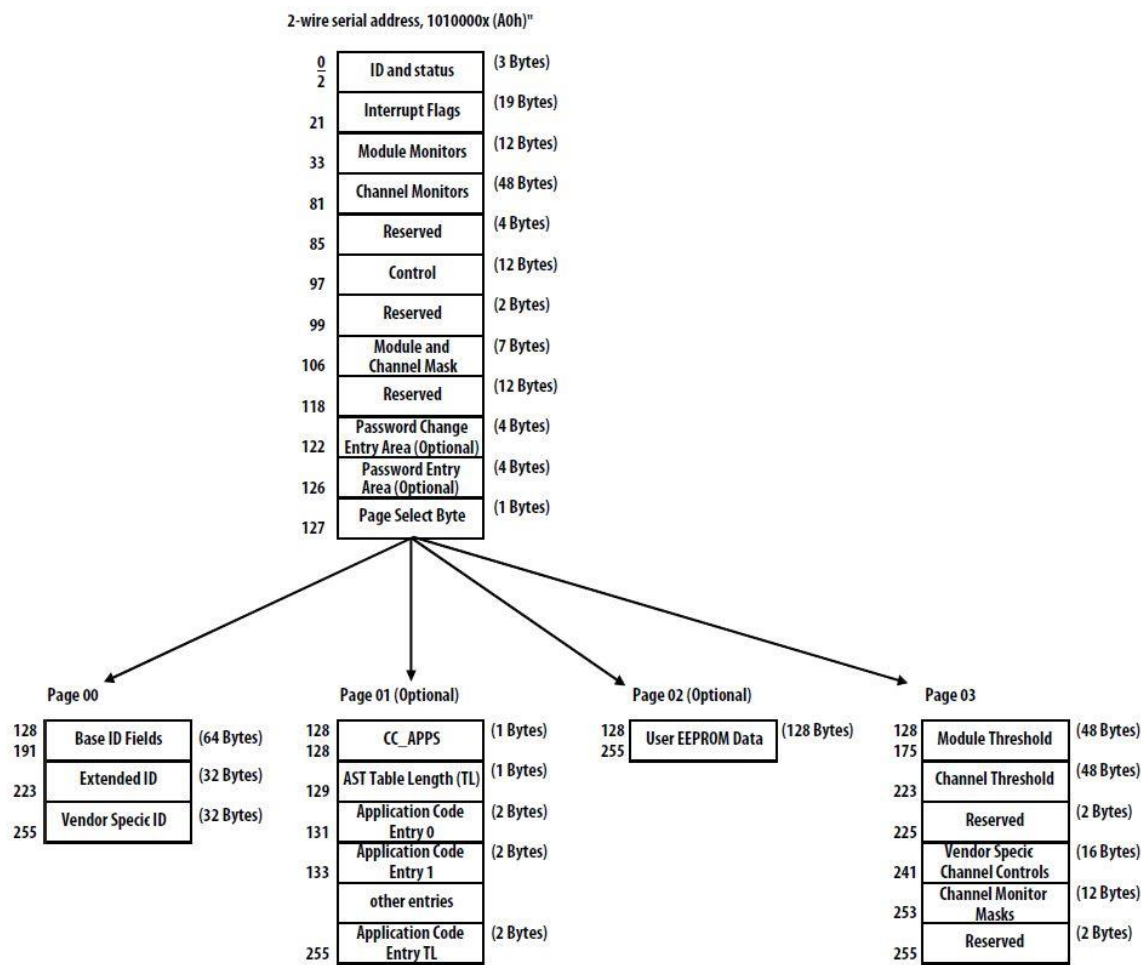


Figure 3. AFBR-79EQDZ Serial Address Page Structure

3.3 Gigabit Ethernet PHY Configuration

The ABCU-5710RZ PHY has 32 16-bit internal registers (Table 8) either read-only or Read/Write that can be accessed by I2C on the address **0x31**.

Table 8. ABCU-5710RZ internal registers mapping (See Data Sheet for details).

| Addr | Hex | ASCII | Addr | Hex | ASCII | Addr | Hex | ASCII | Addr | Hex | ASCII |
|------|-----|-------|------|--------|-------|------|--------|-------|------|--------|-------|
| 0 | 03 | | 40 | 41 | A | 68 | Note 3 | | 96 | Note 5 | |
| 1 | 04 | | 41 | 42 | B | 69 | Note 3 | | 97 | Note 5 | |
| 2 | 00 | | 42 | 43 | C | 70 | Note 3 | | 98 | Note 5 | |
| 3 | 00 | | 43 | 55 | U | 71 | Note 3 | | 99 | Note 5 | |
| 4 | 00 | | 44 | 2D | - | 72 | Note 3 | | 100 | Note 5 | |
| 5 | 00 | | 45 | 35 | 5 | 73 | Note 3 | | 101 | Note 5 | |
| 6 | 08 | | 46 | 37 | 7 | 74 | Note 3 | | 102 | Note 5 | |
| 7 | 00 | | 47 | Note 1 | | 75 | Note 3 | | 103 | Note 5 | |
| 8 | 00 | | 48 | 30 | 0 | 76 | Note 3 | | 104 | Note 5 | |
| 9 | 00 | | 49 | 52 | R | 77 | Note 3 | | 105 | Note 5 | |
| 10 | 00 | | 50 | 5A | Z | 78 | Note 3 | | 106 | Note 5 | |
| 11 | 01 | | 51 | 20 | | 79 | Note 3 | | 107 | Note 5 | |
| 12 | 0D | | 52 | 20 | | 80 | Note 3 | | 108 | Note 5 | |
| 13 | 00 | | 53 | 20 | | 81 | Note 3 | | 109 | Note 5 | |
| 14 | 00 | | 54 | 20 | | 82 | Note 3 | | 110 | Note 5 | |
| 15 | 00 | | 55 | 20 | | 83 | Note 3 | | 111 | Note 5 | |
| 16 | 00 | | 56 | 20 | | 84 | Note 4 | | 112 | Note 5 | |
| 17 | 00 | | 57 | 20 | | 85 | Note 4 | | 113 | Note 5 | |
| 18 | 64 | | 58 | 20 | | 86 | Note 4 | | 114 | Note 5 | |
| 19 | 00 | | 59 | 20 | | 87 | Note 4 | | 115 | Note 5 | |
| 20 | 41 | A | 60 | 00 | | 88 | Note 4 | | 116 | Note 5 | |
| 21 | 56 | V | 61 | 00 | | 89 | Note 4 | | 117 | Note 5 | |
| 22 | 41 | A | 62 | 00 | | 90 | Note 4 | | 118 | Note 5 | |
| 23 | 47 | G | 63 | Note 2 | | 91 | Note 4 | | 119 | Note 5 | |
| 24 | 4F | O | 64 | 00 | | 92 | 00 | | 120 | Note 5 | |
| 25 | 20 | | 65 | 10 | | 93 | 00 | | 121 | Note 5 | |
| 26 | 20 | | 66 | 00 | | 94 | 00 | | 122 | Note 5 | |
| 27 | 20 | | 67 | 00 | | 95 | Note 2 | | 123 | Note 5 | |
| 28 | 20 | | | | | | | | 124 | Note 5 | |
| 29 | 20 | | | | | | | | 125 | Note 5 | |
| 30 | 20 | | | | | | | | 126 | Note 5 | |
| 31 | 20 | | | | | | | | 127 | Note 5 | |
| 32 | 20 | | | | | | | | | | |
| 33 | 20 | | | | | | | | | | |
| 34 | 20 | | | | | | | | | | |
| 35 | 20 | | | | | | | | | | |
| 36 | 01 | | | | | | | | | | |
| 37 | 00 | | | | | | | | | | |
| 38 | 17 | | | | | | | | | | |
| 39 | 6A | | | | | | | | | | |

3.4 Status Led's

There are five status led's that may indicate Loss Of Signal. Table 9 presents LED status description.

Table 9. Led Status Indicators.

| LED | Description | Status |
|-----|---|--|
| E1 | May indicate Loss Of Signal for Ethernet Port (Eth #01) - Connected to Carrier FPGA. | Not Supported by PHY (Always GREEN) |
| E2 | May indicate Loss Of Signal for Ethernet Port (Eth #02) - Connected to Carrier AMC Bay#0. | Not Supported by PHY (Always GREEN) |
| D1 | May indicate Loss Of Signal for Digital optical Port (Optical #01) | GREEN on Normal Operation |
| D2 | May indicate Loss Of Signal for Digital optical Port (Optical #02) | GREEN on Normal Operation |
| D3 | May indicate Loss Of Signal for Digital optical Port (Optical #03) | GREEN on Normal Operation |

[1] AdvancedTCA Rear Transition Module for Physics. PICMG® PhysRTM.0, Revision 1.0 Draft 0.1g, PCI Industrial Computer Manufacturers Group. January 20, 2010.

[2] PICMG: PCI Industrial Computer Manufacturers Group.

[3] AdvancedTCA® Base Specification, PICMG® 3.0, Revision 3.0, PCI Industrial Computer Manufacturers Group. March 24, 2008

[4] Visual information about link OK is provided on the rear panel, through Green Leds.

[5] The Interface refers to ATCA-Carrier-PCIeSW carrier board, developed by IPFN.

[6] AFBR-79EQDZ, 40 Gigabit Ethernet & InfiniBand QSFP+ Pluggable, Parallel Fiber-Optics Module, Avago Technologies.

[7] ABCU-5710RZ / ABCU-5700RZ, 1000BASE-T 1.25 GBd Small Form Pluggable Low Voltage (3.3 V), Electrical Transceiver over Category 5 Cable. Avago Technologies

[8] http://www.nxp.com/products/interface_and_connectivity/i2c/i2c_multiplexers_switches/PCA9548A.html.

[9] http://www.avagotech.com/pages/en/fiber_optics/parallel_optics/4-channel_transceivers/afbr-79eqdz/