Historic

DATE	VERSION	DESCRIPTION	AUTHOR
29-October-2013	1.0	Initial Version	ACombo

Description

The ATCA_PTSW-AMC4_RTM844 is an xTCA[1] based module that follows the specifications presented in PICMG® 3.8, RC1.0f from 2 July 2011 that complements PICMG® 3.0, Revision 3.0 with respect to ARTM[2] specification.

The module provides interface capabilities extension for the ATCA Base carrier.

The module implements the following functions:

- PCI Express 8 lane over cable **upstream port**, compliant with v1.x, operating as a downstream system using ATCA Base carrier with a PCIe bay. The PCIe lanes are mapped on ATCA Base Carrier according Table 2.
- PCI Express 4 lane over cable **upstream port**, compliant with v1.x., operating as a downstream system using ATCA Base carrier with a PCIe bay. The PCIe lanes are mapped on ATCA Base Carrier according Table 3.
- PCI Express 4 lane over cable **downstream port**, compliant with v1.x., operating as a upstream system using ATCA Base carrier with a PCIe bay. The PCIe lanes are mapped on ATCA Base Carrier according Table 4.
- Two Gigabit Ethernet ports that are mapped on ARTM connector according Table 5.
- Three General purpose Optical interfaces using SFP (Small form-factor pluggable) connector. These ports are mapped on ARTM connector according Table 6.
- External timing and trigger features connector.
- The ARTM provides features for control and status of on-board devices that are mapped on the ARTM, according tables referenced above.

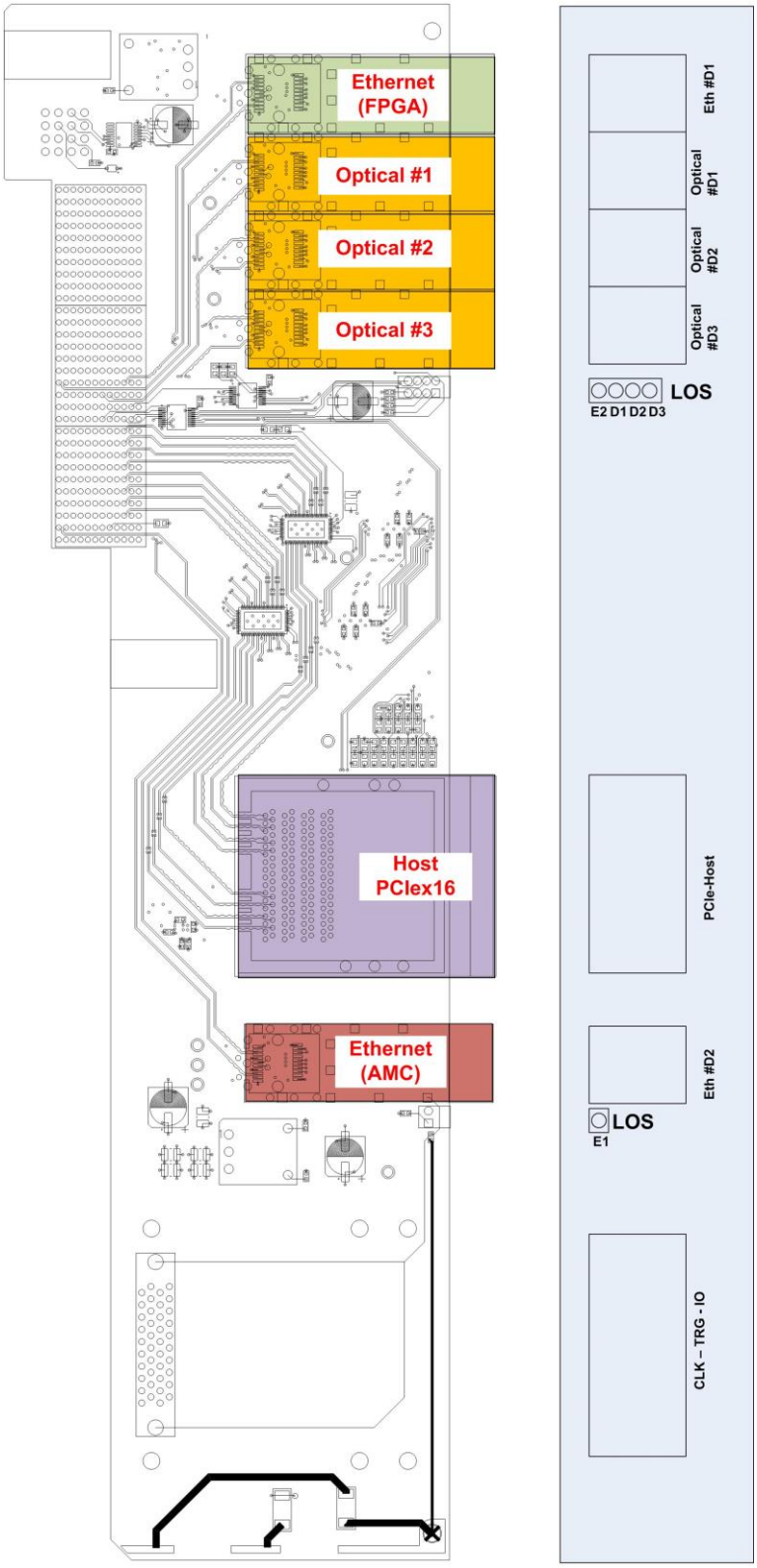

Figure 1. ATCA_PTSW-AMC4_RTM844Diagram.

BOARD INFRASTRUCTURE

ARTM POWER CONNECTOR

This connector follows specifications of AdvancedTCA Rear Transition Module Zone 3A, PICMG® 3.8, RC1.0f from 2 July 2011.

Pin #	Use	Pin #	Use	Pin #	Use	Pin #
A1	MP	A2	MP Rtn	A3	PWR	A4
B1	ENABLE#	B2	PS#[1]	B3	PWR	B4
C1	SCL_L	C2	SDA_L	C3	Reserved	C4
D1	JTAG TCK	D2	JTAG TDO	D3	JTAG TDI	D4

Table 1. Power/Management Connector Pin (see Table 2-1 of specification).

ARTM FABRIC CONNECTORS PINOUT (ATCA -ZONE 3)

The Fabric connector follows AdvancedTCA Rear Transition Module Zone 3A, PICMG® 3.8, RC1.0f from 2 July 2011, that points out to PICMG® 3.3 Revision 3.0 AdvancedTCA® Base Specification and auxiliary documents.

The RP31 ARTM may or may not be assembled. There is no internal connection for this connector.

Table 2. PCI Express over cable 8-lane Upstream Port #A lanes mapping on the ARTM connector.

Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal
Rp33	F1	Port_0_Tx-	Rp33	F2	Port_2_Tx-	Rp33	F3	Port_4_Tx-	Rp33	F4	Port_6_Tx-
Rp33	E1	Port_0_Tx+	Rp33	E2	Port_2_Tx+	Rp33	E3	Port_4_Tx+	Rp33	E4	Port_6_Tx+
Rp33	H1	Port_0_Rx-	Rp33	H2	Port_2_Rx-	Rp33	H3	Port_4_Rx-	Rp33	H4	Port_6_Rx-
Rp33	G1	Port_0_Rx+	Rp33	G2	Port_2_Rx+	Rp33	G3	Port_4_Rx+	Rp33	G4	Port_6_Rx+
Rp33	B1	Port_1_Tx-	Rp33	B2	Port_3_Tx-	Rp33	B3	Port_5_Tx-	Rp33	B4	Port_7_Tx-
Rp33	A1	Port_1_Tx+	Rp33	A2	Port_3_Tx+	Rp33	A3	Port_5_Tx+	Rp33	A4	Port_7_Tx+
Rp33	D1	Port_1_Rx-	Rp33	D2	Port_3_Rx-	Rp33	D3	Port_5_Rx-	Rp33	D4	Port_7_Rx-

Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal
Rp33	C1	Port_1_Rx+	Rp33	C2	Port_3_Rx+	Rp33	C3	Port_5_Rx+	Rp33	C4	Port_7_Rx+
Rp33	F9	dPERST# ([1])	Rp32	F9	PRSNT#(6)	Rp32	E9	WAKE#(6)	Rp32	H9	PWRON(6)
Rp33	H9	RTM_FCLKA-	Rp33	G9	RTM_FCLKA+						

Table 3. PCI Express over cable 4-lane Upstream Port #B lanes mapping on the ARTM connector.

Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal
Rp33	F5	Port_8_Tx-	Rp33	B5	Port_9_Tx-	Rp33	F6	Port_10_Tx-	Rp33	B6	Port_11_Tx-
Rp33	E5	Port_8_Tx+	Rp33	A5	Port_9_Tx+	Rp33	E6	Port_10_Tx+	Rp33	A6	Port_11_Tx+
Rp33	H5	Port_8_Rx-	Rp33	D5	Port_9_Rx-	Rp33	H6	Port_10_Rx-	Rp33	D6	Port_11_Rx-
Rp33	G5	Port_8_Rx+	Rp33	C5	Port_9_Rx+	Rp33	G6	Port_10_Rx+	Rp33	C6	Port_11_Rx+
Rp33	F9	CPERST#(6)	Rp32	F9	PRSNT#(6)	Rp32	E9	WAKE#(6)	Rp32	H9	PWRON(6)
Rp33	H10	RTM_AUX-	Rp33	G10	RTM_AUX+						

Table 4. PCI Express over cable 4-lane Downstream Port #C lanes mapping on the ARTM connector.

Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal	Con	Pin	Signal
Rp33	F7	Port_12_Tx-	Rp33	B7	Port_13_Tx-	Rp33	F8	Port_14_Tx-	Rp33	B8	Port_15_Tx-
Rp33	E7	Port_12_Tx+	Rp33	A7	Port_13_Tx+	Rp33	E8	Port_14_Tx+	Rp33	A8	Port_15_Tx+
Rp33	H7	Port_12_Rx-	Rp33	D7	Port_13_Rx-	Rp33	H8	Port_14_Rx-	Rp33	D8	Port_15_Rx-
Rp33	G7	Port_12_Rx+	Rp33	C7	Port_13_Rx+	Rp33	G8	Port_14_Rx+	Rp33	C8	Port_15_Rx+
Rp33	F9	dPERST#	Rp32	F9	PRSNT#(6)	--	--	WAKE#([2])	--	--	PWRON([3])
Rp33	D10	RTM_TRG-	Rp33	C10	RTM_TRG+						

Table 5. Giga-bit Ethernet mapping (SFP Connector) on the ARTM connector.

Con	Pin	Signal	Description	Interface[4]
Rp33	B9	GbE_Port_0_Tx-	Gigabit Transmit Signal-pair	AMC #1 Site
Rp33	A9	GbE_Port_0_Tx+		

Con	Pin	Signal	Description	Interface[4]
Rp33	D9	GbE_Port_0_Rx-	Gigabit Receiver Signal-pair	
Rp33	C9	GbE_Port_0_Rx+		
Rp32	B9	RTM_SFP_TX_DISABLE_1	SFP Transmit Disable	
Rp32	A9	RTM_SFP_LOS_1	SFP Loss of Signal (*)	
Rp32	F7	GbE_Port_1_Tx-	Gigabit Transmit Signal-pair	FPGA Ethernet Port #0
Rp32	E7	GbE_Port_1_Tx+		
Rp32	H7	GbE_Port_1_Rx-	Gigabit Receiver Signal-pair	
Rp32	G7	GbE_Port_1_Rx+		
Rp32	D9	RTM_SFP_TX_DISABLE_2	SFP Transmit Disable	
Rp32	C9	RTM_SFP_LOS_3	SFP Loss of Signal (*)	

(*)Depending on SFP connector used, this signal may not be used.

Table 6. Optical SFP connector mapping on the ARTM connector.

Con	Pin	Signal	Description	Interface6
Rp32	B7	IO _Port_1_Tx-	Transmit Signal-pair	FPGA MGT Port #?
Rp32	A7	IO _Port_1_Tx+		
Rp32	D7	IO _Port_1_Rx-	Receiver Signal-pair	
Rp32	C7	IO _Port_1_Rx+		
Rp32	F10	RTM_SFP_TX_DISABLE_3	SFP Transmit Disable	
Rp32	E10	RTM_SFP_LOS_3	SFP Loss of Signal (*)	
Rp32	F8	IO _Port_2_Tx-	Transmit Signal-pair	FPGA MGT Port #?
Rp32	E8	IO _Port_2_Tx+		
Rp32	H8	IO _Port_2_Rx-	Receiver Signal-pair	
Rp32	G8	IO _Port_2_Rx+		
Rp32	H10	RTM_SFP_TX_DISABLE_4	SFP Transmit Disable	
Rp32	G10	RTM_SFP_LOS_4	SFP Loss of Signal (*)	
Rp32	B8	IO _Port_3_Tx-	Transmit Signal-pair	FPGA MGT Port #?
Rp32	A8	IO _Port_3_Tx+		
Rp32	D8	IO _Port_3_Rx-	Receiver Signal-pair	
Rp32	C8	IO _Port_3_Rx+		
Rp32	B10	RTM_SFP_TX_DISABLE_5	SFP Transmit Disable	

Rp32	A10	RTM_SFP_LOS_5	SFP Loss of Signal (*)	

(*) Depending on SFP connector used, this signal may not be used.

Table 7. Clock, Trigger and user defined signals mapping on the ARTM connector.

Con	Pin	Signal	Description	Interface6
Rp33	F10	RTM_CLK-	External Clock	FPGA I/O – TCLKB
Rp33	E10	RTM_CLK+		
Rp33	B10	RTM_IRIG-	IRIG Time Code	FPGA I/O – TCLKD
Rp33	A10	RTM_ IRIG +		
Rp32	G9	RTM_SIGNAL	User defined	FPGA I/O
Rp32	D10	RTM_SPAREIO-	User defined	
Rp32	C10	RTM_SPAREIO+		

PCIE HOST CONNECTORS

The ATCA_PTSW-AMC4_RTM844 Module has an iPass™ Connector [5] from Molex that is qualified for using with PCIex8 and PCIex4.

The PCIe ports are mapped into ARTM fabric connector as depicted in Table 2, Table 3 and Table 4.

The ATCA_PTSW-AMC4_RTM844 Module includes re-drivers in the PCI-e lanes and in the clock distribution from Host.

PCIE RE-DRIVERS

The PCIe re-drivers (National Semiconductors® DS50PCI402) can be configured for optimization regarding actual physical system conditions. A detailed description can be found at http://www.national.com/ds/DS/DS50PCI402.pdf.

Table 8 and Table 9 present the possible settings for Equalization of the input signals and De-Emphasis of output signals. The settings are programmed by assembling or not some resistors. The tables present the required resistors that MUST be assembled in order to get the selected option. The default option is put in evidence.

The De-Emphasis settings are Rate dependent and may be configured through R100 and R101 (see Table 10).

Table 8. Equalization Configuration Pins for the re-drivers B ports (3-level input: ‘0’, ‘1’, ‘Float’).

EQ1	EQ0	RP33 Side		Cable Side		EQ Gain 1.25 GHz (dB)	EQ Gain 2.5 GHz (dB)	Suggested Use
		EQ1	EQ0	EQ1	EQ0			
F	F					0	0	Bypass
1	1	R103	R105	R107	R109	2.6	5.0	8" FR4 (6-mil trace) or < 1m (28 AWG) PCIe cable
0	0	R102	R104	R106	R108	3.8	7.6	14" FR4 (6-mil trace) or 1m (28 AWG) PCIe cable
F	0		R104		R108	6.4	11.6	20" FR4 (6-mil trace) or 5m (26 AWG) PCIe cable
1	0	R103	R104	R107	R108	8.5	15.6	30" FR4 (6-mil trace) or 7m (24 AWG) PCIe cable
F	1		R105		R109	11.3	17.5	40" FR4 (6-mil trace) or 9m (24 AWG) PCIe cable
0	1	R102	R105	R106	R109	12.8	19.8	50" FR4 (6-mil trace) or 10m (24 AWG) PCIe cable
0	F	R102		R106		12.4	21.3	15m (24 AWG) PCIe cable
1	F	R103		R107		18.1	27.2	> 15m (24 AWG) PCIe cable

Table 9. De-Emphasis Configuration Pins for the re-driver ports (3-level input: ‘0’, ‘1’, ‘Float’).

DEM1	DEM0	RP33 Side		Cable Side		De-Emphasis (dB)	VOD (V)	Suggested Use @ Rate = 2.5GHz
		DEM1	DEM0	DEM1	DEM0			
0	0	R114	R116	R110	R112	0dB	1	
0	1	R114	R117	R110	R113	-3.5dB	1	8 inches FR4 (6-mil trace) or less than 1 meter (28 AWG) PCIe cable
1	0	R115	R116	R111	R112	-6dB	1	
1	1	R115	R117	R111	R113	-6dB	1	15 inches FR4 (6-mil trace)
0	F	R114		R110		-9dB	1	
1	F	R115		R111		-12dB	1	
F	0		R116		R112	-9dB	1.2	30 inches FR4 (6-mil trace)
F	1		R117		R113	-12dB	1.4	40 inches FR4 (6-mil trace)

Table 10. Other Configuration Pins for the re-drivers.

Signal Name	Options	Description
RATE		Rate is internally detected.
	R100	Forces Gen1 (2.5Gbps).
	R101	Forces Gen2 (5Gbps).
SD_TH	R128, R129, R130, R131	Threshold select pin for electrical idle detect threshold. Float pin for default 130mV DIFF p-p, otherwise connect resistor from SD_TH to GND to set threshold voltage (See Data Sheet). Default: FLOAT.

PCIE CABLE SIDEBAND SIGNALS

According to PCI Express External Cabling Specification, Rev. 1.0 (Jan. 4, 2007) the implementation of cabled PCIe, requires a set of sideband signals. ATCA_PTSW-AMC4_RTM844 implements the management of these signals for full compliance with the standard.

- **CREFCLK (required)**: Upstream ports have buffered clocks transmitted to the ATCA carrier board. Downstream port receives a reference clock from the ATCA carrier buffered in the RTM card. (See Table 2, Table 3 and Table 4.)
- **CPRSNT# (required)**: This signal is must be provided by the ATCA carrier and is broadcasted to ALL upstream systems.
- **CPERST# (required)**: This signal provides a Reset from ANY Upstream system to the ATCA carrier. ANY Upstream system MAY activate this signal.
- **CPWRON (required)**: This is a notification from the upstream system for the downstream system turn the power ON. Note that the notification is received on the FIRST Upstream command.
- **SB_RTN (required)**: This is the return current path for Upstream system signals. This is required for keeping subsystems power isolation.
- **CWAKE# (required)**: This signal is driven by the ATCA carrier and supports the wakeup funcionailty
- **+3.3 V POWER (optional for connector)**: Not used in ATCA_PTSW-AMC4_RTM844.
- **PWR_RTN (optional for connector)**: Not used in ATCA_PTSW-AMC4_RTM844.

GIGABIT ETHERNET CONNECTORS

The ATCA_PTSW-AMC4_RTM844Module has two 1000BASE-T 1.25 GBd Small Form Pluggable (SFP) electrical transceivers over Category 5 Cable. The transceivers used are ABCU-5710RZ[6] from Avago Technologies.

These Ethernet ports are mapped into ARTM fabric connector as depicted in Table 5.

GIGABIT OPTICAL CONNECTORS

The ATCA_PTSW-AMC4_RTM844 Module has three Short-Wavelength Pluggable (SFP) Transceivers from Finisar, capable of up to 1.25 Gb/s duplex with a 850 nm VCSEL laser transmitter.

These Gigabit Optical ports are mapped into ARTM fabric connector as depicted in Table 6.

CLOCK, TRIGGER AND GPIO CONNECTOR

The ATCA_PTSW-AMC4_RTM844 Module includes a connector that may be used for the distribution of several clock signal and general purpose signals. The following table presents the connector pinout.

Table 11. Clock and General purpose Connector pinout (J7).

Pin	Signal	Description
1	RTM_TRG-	External Trigger
3	RTM_TRG+	
5	RTM_IRIG-	IRIG Time Code
7	RTM_ IRIG +	
9	RTM_AUX-	User defined
11	RTM_ AUX +	
13	RTM_CLK-	External Clock
15	RTM_CLK+	
17	RTM_SPAREIO-	User defined
19	RTM_SPAREIO+	
40	SIGNAL	User defined
2, 4, 6, 8, 10, 12, 14, 16, 18, 20	GND	Ground
22, 24	RTM_12V	RTM 12V Power.
26, 28	RTM_3V	RTM 3.3V Power.
30, 32	3V3	Adjustable power supply (Default 3.3V)
34, 36	VTD25	RTM 2.5V Power.

CONFIGURATION SETTINGS AND STATUS

Configurations of ATCA_PTSW-AMC4_RTM844 module are limited to transmitter/receiver connector/chipsets where protocol and/or physical operation condition may be changed. In addition some features may be used to identify installed infrastructure. The

configuration is performed trough the Power and Management plug on Zone 3 (see Table 1).

Status will be available through Led's on rear panel and on Zone 3 Data Connectors as presented on Table 14.

GENERAL CONFIGURATION

The ARTM configuration uses I2C protocol at address 0x70. The ARTM has two internal devices that may require configuration, which are the two Gigabit Ethernet ports. The access and configuration must be supported by the ATCA Host Board.

Table 12 presents the mapping for the I2C switch (PC9546A from NXP Semiconductors®) with the indication of Control bit register (Figure 2) that enables each port. For detailed information regarding I2C switch PC9546A data sheet must be consulted.

Table 12. Mapping of ARTM I2C devices into PC9546A ports.

PC9546A Port	**Control Register bit**	**ARTM Device**
Port #0	Bit-0	Ethernet Port (Connected to Carrier AMC Bay #0)
Port #1	Bit-1	Ethernet Port (Connected to Carrier FPGA)
Port #2	Bit-2	Not Used
Port #3	Bit-3	Not Used

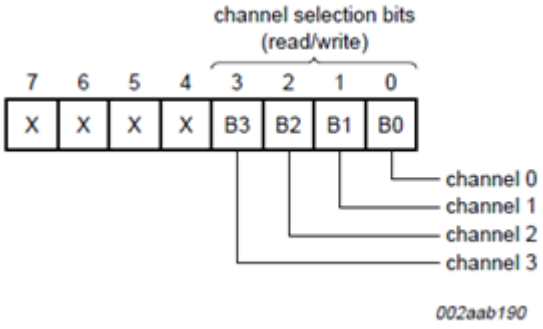

Figure 2. PC9546A Control bit Register.

GIGABIT ETHERNET PHY CONFIGURATION

The ABCU-5710RZ PHY has 32 16-bit internal registers (Table 13) either read-only or Read/Write that can be accessed by I2C on the address 0x31.

Table 13. Mapping of ARTM I2C devices into PC9546A ports (see 8).

Addr	Hex	ASCII	Addr	Hex	ASCII	Addr	Hex	ASCII	Addr	Hex	ASCII
0	03		40	41	A	68	Note 3		96	Note 5	
1	04		41	42	B	69	Note 3		97	Note 5	
2	00		42	43	C	70	Note 3		98	Note 5	
3	00		43	55	U	71	Note 3		99	Note 5	
4	00		44	2D	-	72	Note 3		100	Note 5	
5	00		45	35	5	73	Note 3		101	Note 5	
6	08		46	37	7	74	Note 3		102	Note 5	
7	00		47	Note 1		75	Note 3		103	Note 5	
8	00		48	30	0	76	Note 3		104	Note 5	
9	00		49	52	R	77	Note 3		105	Note 5	
10	00		50	5A	Z	78	Note 3		106	Note 5	
11	01		51	20		79	Note 3		107	Note 5	
12	0D		52	20		80	Note 3		108	Note 5	
13	00		53	20		81	Note 3		109	Note 5	
14	00		54	20		82	Note 3		110	Note 5	
15	00		55	20		83	Note 3		111	Note 5	
16	00		56	20		84	Note 4		112	Note 5	
17	00		57	20		85	Note 4		113	Note 5	
18	64		58	20		86	Note 4		114	Note 5	
19	00		59	20		87	Note 4		115	Note 5	
20	41	A	60	00		88	Note 4		116	Note 5	
21	56	V	61	00		89	Note 4		117	Note 5	
22	41	A	62	00		90	Note 4		118	Note 5	
23	47	G	63	Note 2		91	Note 4		119	Note 5	
24	4F	O	64	00		92	00		120	Note 5	
25	20		65	10		93	00		121	Note 5	
26	20		66	00		94	00		122	Note 5	
27	20		67	00		95	Note 2		123	Note 5	
28	20								124	Note 5	
29	20								125	Note 5	
30	20								126	Note 5	
31	20								127	Note 5	
32	20										
33	20										
34	20										
35	20										
36	01										
37	00										
38	17										
39	6A										

STATUS LED’S

There are five status led’s that may indicate Loss Of Signal. Table 14 presents LED status description.

Table 14. Led Status Indicators.

LED	Description	Status
E1	May indicate Loss Of Signal for Ethernet Port (Eth #01) - Connected to Carrier FPGA.	Not Supported by PHY (Always GREEN)
E2	May indicate Loss Of Signal for Ethernet Port (Eth #02) - Connected to Carrier AMC Bay#0.	Not Supported by PHY (Always GREEN)
D1	May indicate Loss Of Signal for Digital optical Port (Optical #01)	GREEN on Normal Operation
D2	May indicate Loss Of Signal for Digital optical Port (Optical #02)	GREEN on Normal Operation
D3	May indicate Loss Of Signal for Digital optical Port (Optical #03)	GREEN on Normal Operation

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[1] These signals are shared among Port #A and Port #B and Port #C. They are bidirectional and **require** correct setting on ATCA carrier for proper operation and damage avoiding.

[2] This signal is NOT CONNECTED in RTM card.

[3] This signal is pulled HI (3.3V) in RTM card.

[4] The Interface refers to ATCA-Carrier-PCIeSW carrier board, developed by IPFN.

[5] Connector references are: 75586-0002 (8-lane); 0755860010 (4-lane).

[6] ABCU-5710RZ / ABCU-5700RZ, 1000BASE-T 1.25 GBd Small Form Pluggable Low Voltage (3.3 V), Electrical Transceiver over Category 5 Cable. Avago Technologies

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[1] AdvancedTCA Rear Transition Module for Physics. PICMG® 3.8, RC1.0f from 2 July 2011.

[2] AdvancedTCA® Base Specification, PICMG® 3.0, Revision 3.0, PCI Industrial Computer Manufacturers Group. March 24, 2008.