

Amendment of the service contract ITER/CT/09/10001533

Adaptation and extension of the Fast Plant System Data Acquisition Prototypes

Technical Specifications

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1 Abstract

A first task aimed at designing and implementing two Fast Plant System Controller prototypes specialised for data acquisition, constrained by ITER technology standard decisions and based on 2 different form factors: ATCA and PXIe.

The current amendment intends to start creating high quality products from this initial concept and design phase in order for IO CODAC to integrate them in its catalogue of supported I&C hardware solutions. The products foreseen are:

- ATCA PCIe switch Card – more specifically the RTM PCIe Host Interface,
- ATCA ADC module with the capability to operate either in chopper or in normal mode,
- ATCA shelf with full-mesh interconnection,
- MARTe framework integration preparation in CODAC Core System. The decision of integrating MARTe in CODAC standard solutions is not acted for now. This step is a prerequisite for this decision,
- FlexRIO EPICS ASYN device support for CODAC Core System V3.

2 Background and Objectives

In order to integrate a product into CODAC catalogue of supported solutions, the following stages should be achieved after the conception and design phases:

- Realise:
 - Plan manufacturing
 - Manufacture,
 - Build/Assemble,
 - Test (quality check).
- Service:
 - Sell and Deliver world-wide,
 - Use,
 - Maintain and Support.

The objective of this amendment is to be ready for the production phase. For achieve this step, the products should first be manufactured in small quantities and include the software support (Linux driver and EPICS device support, versioning in SVN, Linux RPM package for automatic installation), as well as the documentation, test plan and samples to be installed and validated by different labs. The following small quantities should be demonstrated for the end of the year:

- 3 x ATCA PCIe switch Cards,
- 2 x ATCA ADC modules,
- 1 x ATCA shelf with full-mesh interconnection specification,
- 1 x MARTe package,
- 1 x FlexRIO EPICS ASYN package.

The realisation and service phases are out of scope of this amendment but a production plan should be demonstrated and its progress will be stated. In particular the price per unit should be estimated and negotiated with IO.

3 Scope of Work

One major goal of this task is to focus on some products extracted from the previous delivered prototypes, and to setup the necessary actions in order to integrate them as standard solutions in CODAC I&C hardware catalogue and CODAC Core System software distribution.

4 Estimated Duration

~8 months starting on beginning of October 2011 and ending in May 2011.

5 Work Description

5.1 Operating Environment

The products will operate on Red Hat Enterprise Linux 64-bits platform version 6. For real time requirements, a tuning on Red Hat MRG extension will be required.

The software environment and samples will be developed using Core System V2.1 distribution.

5.2 Design and Implementation Constraints

The dependency between the products will be minimal in order to use each product in many different configurations. For instance the software support of I/O modules should not rely exclusively on the MARTe module which is only one specific use case. Same remark applies for the FlexRIO EPICS ASYN support device that should not be dependant of any archive or communication system.

5.3 User Documentation

Final engineering and design documents will be delivered for each product as well as the installation and user manuals. For existing products, current material could be referenced and the provided documentation could only focus on CODAC integration and usage.

The source code of each product will be organised according to CODAC standard file structure [IDM: [33T8LW](#)] and will be registered in [CODAC SVN repository](#). The project will be built and managed using the mvn commands: mvn compile, mvn run, mvn stop and mvn package in order to produce RPM packages and ease the deployment process.

A test plan will be produced for each product detailing the different scenarios with the expected results. A monitoring screen based on CSS BOY and EPICS will be developed allowing user interaction. The interface with the alarm server and the archive engine will also be demonstrated using CSS tools. The user will be allowed to change EPICS standard thresholds such as noise reduction, monitor and archive dead bands.

5.4 Assumptions and Dependencies

CODAC will propose a standardisation of FPGA Application Register Table and an abstract model for FPGA Asyn device support which will be provided to implement FlexRIO driver.

Open licensing model will be established for the products allowing all vendors to adhere and access blueprints and code according to the EURATOM licensing.

5.5 Product features

5.5.1 ATCA PCIe switch Card

The product ATCA PCIe switch Card as defined in [ITER_D_3ZH94V](#) will support CODAC TCN architecture and functions.

Time and synchronization on the PCIe switch card will use the absolute time in IRIG format and have a disciplined oscillator servo with 50 ns RMS of phase precision and accuracy (to be discussed during the kick-off meeting).

The product will be xTCA compatible – more specifically μ TCA.4.

In early phase, 3 x ATCA PCIe switch Cards will be shipped to CODAC on site.

5.5.2 ATCA ADC module

The ATCA ADC module as defined in [ITER_D_3ZH94V](#) will be PICMG® 3.0/3.4 compliant and designed for high availability and reliability with easy hot-plug (connectivity on a passive RTM).

The software support of the ATCA ADC product will be independent of MARTe.

In early phase, 2 x ATCA ADC modules will be shipped to CODAC on site.

5.5.3 ATCA shelf

An ATCA commercial shelf that allows interconnection in a full-mesh topology will be selected. World wide support of this product will be required.

5.5.4 MARTe framework integration in CODAC Core System

MARTe framework will be integrated in CODAC SVN repository and deployed as a RPM package. Samples will demonstrate the interface with EPICS and CSS tools.

MARTe framework will allow the production of “processed” signals and related EPICS PVs. It will be possible to setup EPICS thresholds on processed and physical signals.

For instance, alarm monitors will be invoked if the alarm status or severity has changed – for analogue value, alarm status is changed when the hysteresis condition (EPICS field HYST) - dead band around the alarm limits, is met. Archive and value change monitors will be invoked if EPICS field ADEL – archive dead band, and EPICS field MDEL – monitoring dead band, conditions are met.

The EPICS Analogue Input record has also a smoothing filter to reduce noise on the input signal (EPICS field SMOO). This field will also apply to a processed signal by MARTe.

5.5.5 FlexRIO EPICS ASYN generic device support

FlexRIO EPICS ASYN generic device support will be implemented according an abstract model provided by CODAC.

6 Responsibilities (including customs and other logistics)

ITER CODAC will provide CORE System V2.1 and the SVN repository infrastructure.

The contractor will deliver the products that will be installed by ITER CODAC in CODAC infrastructure and tested with the provided documentation.

7 List of deliverables and due dates (proposed or required by ITER)

The contract amendment shall span over a period not more than 8 months (32 weeks), from kick-off to delivery of the final results. Key milestones are:

Milestone and <i>Bidder Deliverables</i>	Dates (weeks)	Location, Action and <i>ITER-IO Deliverables</i>
Kick-off meeting	T ₀	At start of contract (T ₀). This meeting shall be held at ITER IO premises in Cadarache or via phone conference. Detailed schedule and scope shall be agreed. <i>Minutes of Meeting.</i>
Progress meeting <i>Progress Report</i>	Every 4 weeks	These meetings shall be held at ITER IO premises or via phone conference. <i>Minutes of Meeting.</i>
Delivery of the final <i>Engineering Design Document</i>	T ₀ +2 weeks	These documents shall be delivered electronically.
Review	T ₀ +4 weeks	These documents shall be commented by ITER IO. The bidder shall incorporate comments in the next version. <i>Review Report.</i>
Delivery of <i>ICD</i> and <i>Test Plan</i> Delivery of <i>Production Plan</i> (unit cost estimation)	T ₀ +5 weeks	These documents shall be delivered electronically.
Review	T ₀ +7 weeks	These documents shall be commented by ITER IO. The bidder shall incorporate comments in the next version. <i>Review Report.</i>
Delivery of the <i>products</i> with their engineering design documents, <i>test plan</i> and <i>samples</i>	T ₀ +12 weeks	The products will be shipped to ITER IO. The code source and samples will be delivered in SVN. These documents shall be delivered electronically.
Improvement of the product quality	T ₀ +30 weeks	Iterative process. Integration of IO comments and submitted bugs. <i>Monthly Bugs Report.</i>
Delivery of all <i>final documentation and samples</i> for the products	T ₀ +32 weeks	Finalisation. <i>End of task</i>

8 Acceptance Criteria (including rules and criteria)

Each product will be manufactured in small quantity early in the project: this includes hardware and software delivery (Linux driver, EPICS device support, samples). Each product will be tested according to the delivered test plan. This is an iterative process in order to improve the product quality.

9 Specific requirements and conditions

No visit on site is required.

10 Work Monitoring / Meeting Schedule

Progress reports shall be submitted by the Consultant to ITER-IO every four weeks. Each progress report shall summarise the work done during the reporting period and describe any problems encountered. The progress report shall be delivered 3 working days before the corresponding progress meeting.

Minutes of meetings and review reports, including action item lists, shall be written by ITER-IO and drafts shall be sent to the Bidder by e-mail not later than 3 days after the meeting. After agreement by the Bidder, by e-mail, the minutes of meeting and review reports shall be released.

11 Payment schedule / Cost and delivery time breakdown

Milestone	Dates (weeks)	Payment condition
Kick-off meeting	T ₀	20% <i>Minutes of the kick-off Meeting.</i>
Delivery of the <i>products</i> with their engineering design documents, <i>test plan</i> and <i>samples</i>	T ₀ +12 weeks	40% <i>Review Report.</i>
Delivery of all <i>final documentation</i> and <i>software</i> for the products	T ₀ +32 weeks	40% <i>Post Mortem Analysis Report.</i>

12 Quality Assurance (QA) requirement

The general requirements are detailed in ITER document [ITER Procurement Quality Requirements \(22MFG4\)](#).

Prior to commencement of the task, a Quality Plan [Quality Plan \(22MFMW\)](#) must be submitted for IO approval giving evidence of the above and describing the organisation for this task; the skill of workers involved in the study; any anticipated sub-contractors; and giving details of who will be the independent checker of the activities.

Prior to commencement of any manufacturing, a Manufacturing & Inspection Plan [Manufacturing and Inspection Plan \(22MDZD\)](#) must be approved by ITER who will mark up any planned interventions.

Deviations and Non-conformities will follow the procedure detailed in IO document [MQP Deviations and Non Conformities \(22F53X\)](#)

Prior to delivery of any manufactured items to the IO Site, a Release Note must be signed [MQP Contractors Release Note \(22F52F\)](#).

Documentation developed as the result of this task shall be retained by the performer of the task or the DA organization for a minimum of 5 years and then may be discarded at the direction of the IO. The use of computer software to perform a safety basis task activity such as analysis and/or modelling, etc shall be reviewed and approved by the IO prior to its use, it should fulfil IO document on Quality Assurance for ITER Safety Codes [Quality Assurance for ITER Safety Codes \(258LKL\)](#).

13 References / Terminology and Acronyms

ADC	Analogue to Digital Converter
ATCA	Advanced Telecommunications Computing Architecture
CODAC	Control , Data Access and Communication
COTS	Commercial Off The Shelf
CPU	Central Processing Unit
DAC	Digital to Analogue Converter
DIO	Digital Input Output
I/O	Input/Output
I&C	Instrumentation and Control
ITER-IO	ITER International Organization
N/A	Not Applicable
NIC	Network Interface Card
OS	Operating System
PCle	Peripheral Component Interconnect Express
PLC	Programmable Logical Controller
PSH	Plant System Host
PXI	PCI eXtension for Instrumentation
RTOS	Real-time Operating System
TBD	To Be Defined